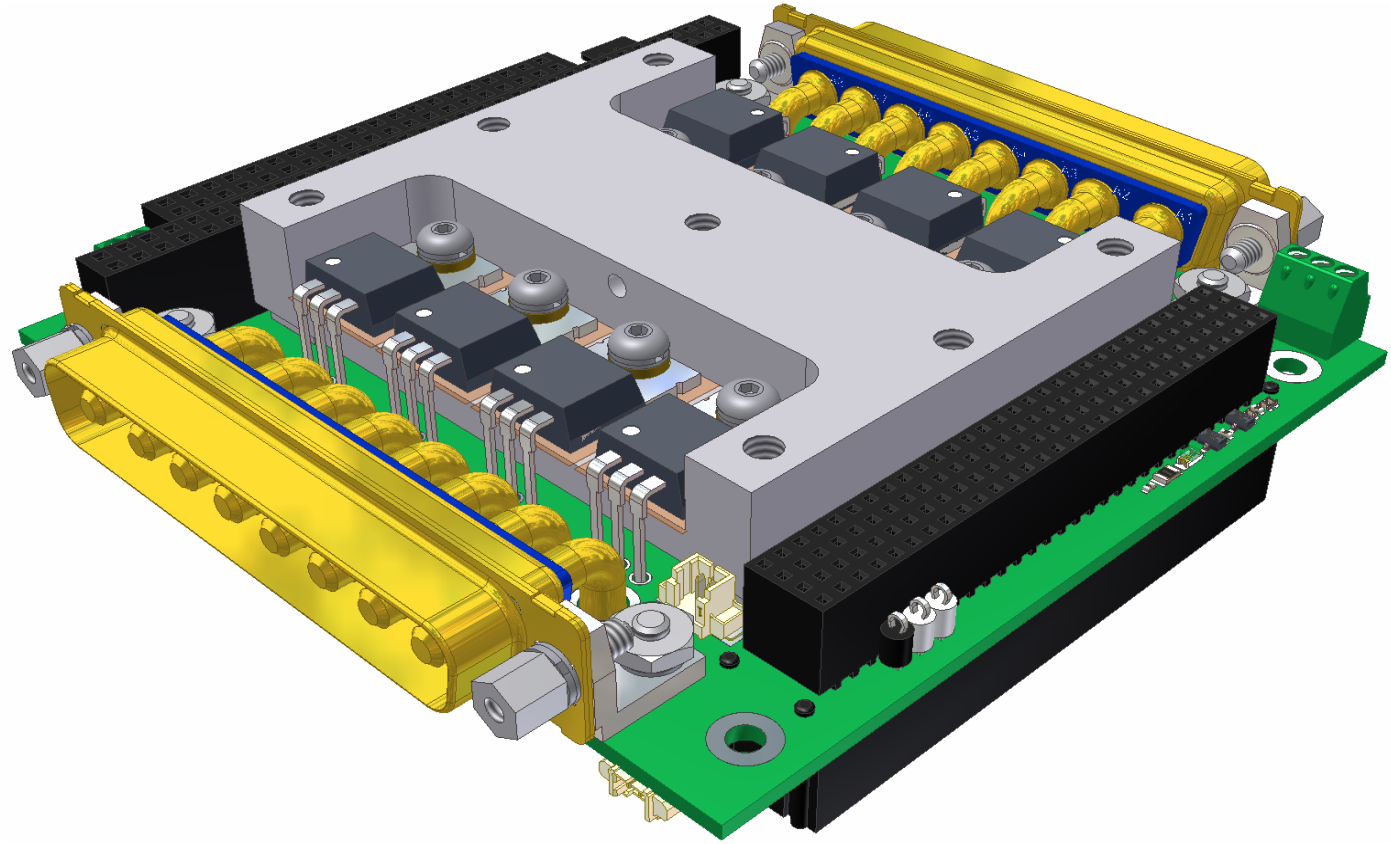
LAKENHEATH ELECTRONICS DESIGN

Compact Power Control

PB8000 PC/104 8-CHANNEL POWER SWITCH



USER MANUAL

Rev 1.2

Lakenheath Electronics Design, Inc. * Bethesda * MD * 20814 * USA
Phone: 301.404.0386 **World Wide Web:** www.lakenheathelectronics.com

Notice

The information in this document is provided for reference only. Lakenheath Electronics Design does not assume any liability arising out of the application or use of the information or products described herein. This document may contain or reference information and products protected by copyrights or patents and does not convey any license under the patent rights of Lakenheath Electronics Design, nor the rights of others.

WARNING!!

TURN SYSTEM POWER OFF BEFORE INSTALLING THIS PRODUCT. CONNECTING AND DISCONNECTING CABLES FROM THIS PRODUCT OR INSTALLING THIS PRODUCT INTO A POWERED SYSTEM MAY CAUSE DAMAGE TO THIS PRODUCT AND WILL VOID ALL WARRANTIES, IMPLIED OR EXPRESSED.

Warranty

Lakenheath Electronics Design's products are thoroughly inspected and tested prior to shipment and are warranted to be free of defects in workmanship and material. Under this warranty, Lakenheath Electronics Design shall provide repair or replacement parts without charge (except shipping charges) to correct any defects which appear within 12 months from the date of shipment. Extended warranty periods may apply for OEM contracts (quantities 100+). Any claim under this warranty must be in writing and received by Lakenheath Electronics Design within 30 days prior to the end of the warranty period or within 30 days of the discovery of the defect, whichever occurs first. This warranty is contingent upon proper use of the products and will be void in the event of unauthorized repair or any modification other than such modification described in original manufacturer's and/or Lakenheath Electronics Design's guidelines and documentation

The following will void the Warranty:

- Damages due to improper handling (Non-ESD Safe Environment).
- Units, where the serial number has been destroyed or taken away.
- Any damage that is the result of not following the directions. Non-Warranty Damage can occur from (but is not limited to) the following examples: power or peripheral cables not properly connected (installed off by one row, installed backwards, bent or broken pins, etc.), using defective or misconnected boards in the PC/104 stack, applying improper voltages to the board, exceeding the thermal or electrical specifications of this product, careless handling of the product and damage from electrical shorts due to improperly grounded tools or peripherals.
- Physical damage to the board.

Any units that have to be sent back to Lakenheath Electronics Design for repair require an RMA number which can be obtained by either calling our Technical Support department at 301 404-0386 or via e-mail to TechnicalSupport@LakenheathElectronics.com.

Lakenheath Electronics Design reserves the right to change the specifications contained in this document without notice.

TABLE OF CONTENTS

Section **Title** **Page**

RECORD OF CHANGES

Section **Title** **Page**

REVISION	DATE	TITLE OR BRIEF DESCRIPTION	ENTERED BY
1.0	08/12/06	Initial release	T. Seeley
1.1	08/13/06	Digital Temperature Sensor section added to Appendix B	T. Seeley
1.2	08/15/06	Added Section 3.0 Specifications Added Section 4.0 Structural Heat Sink	T. Seeley

LIST OF FIGURES

Section **Title** **Page**

LIST OF TABLES

1.0. INTRODUCTION

1.1. Product Description.

With the PB8000 PC/104 8-Channel Power Switch, the user benefits from having eight, optically-isolated power MOSFETs capable of switching 20A (or more) each in a form-factor suitable for embedded PC/104 or PC/104 *Plus* systems. Although designed to stack with other PC/104 modules in an embedded system where control of the device is via the PC/104 ISA bus, the device can also be operated in a "stand-alone" configuration over an RS485 serial link or an 8-bit bus (plus an enable and a strobe). An interface for operating the MOSFET power channels with discrete commands coming from external toggle or pushbutton switches is also built in. External LED indicators for power channel status are supported. The aluminum MOSFET heat spreader is outfitted with seven, 8-32 tapped holes for attaching the heat spreader to a structural heat sink. The temperature of the heat spreader is easily monitored with an included thermistor. A digital temperature sensor is also provided to monitor heat spreader temperature under software control. Onboard soft-start circuitry helps manage inrush current to connected loads.

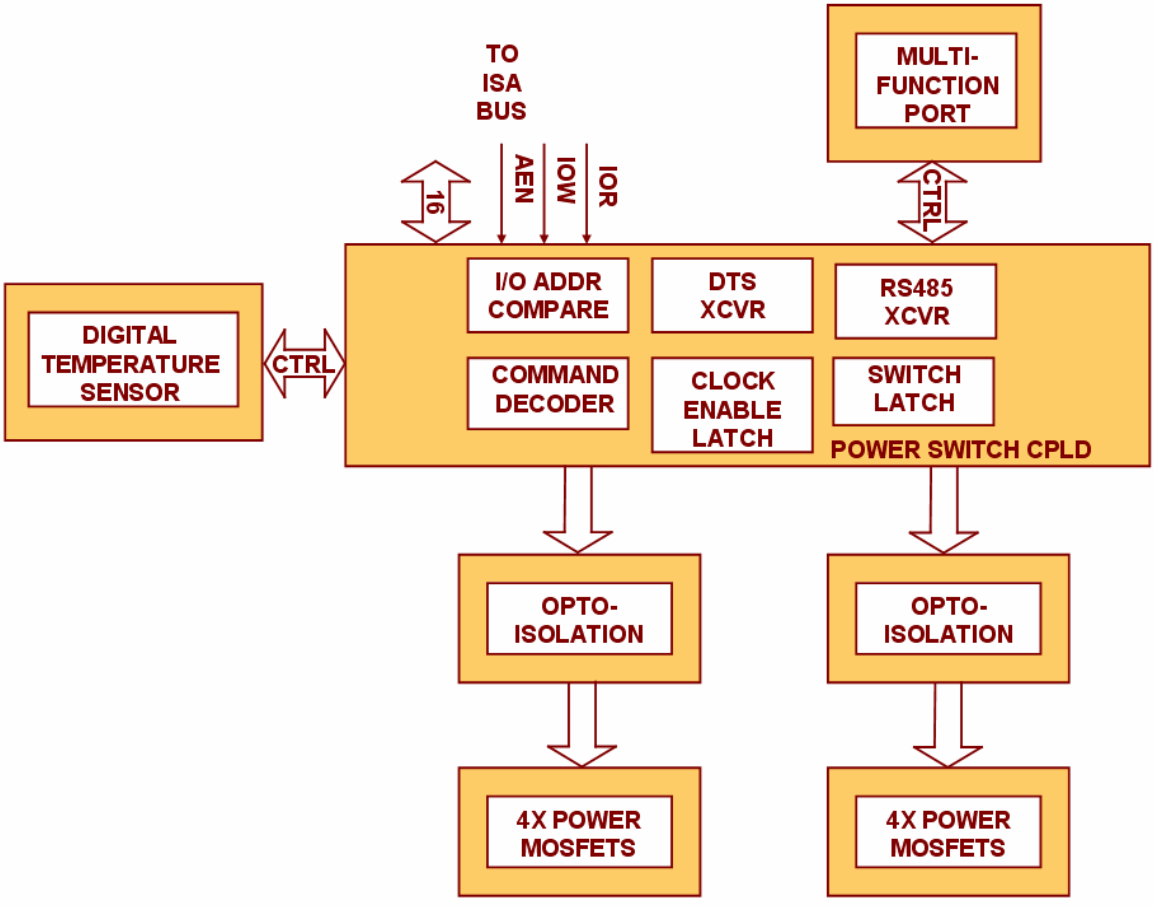


Figure 1-1. Block Diagram: 8-Channel Power Switch.

Figure 1-1 is a simplified block diagram of the PB8000. When mounted in a PC/104 stack, control is provided over the ISA bus. (Note: Although a PCI connector (J5) is installed, this connector functions as a “pass-thru” connector for situations where the PB8000 is installed in a PC/104 *Plus* stack.) In a “stand-alone” configuration, control is provided through the multi-function port. The multi-function port can serve as an RS485 interface, an 8-bit bus interface (plus enable and strobe), a toggle switch interface, a push-button interface and a JTAG interface (for firmware upload). Access to the digital temperature sensor is via the ISA bus or the RS485 interface only.

1.2. Connector Locations.

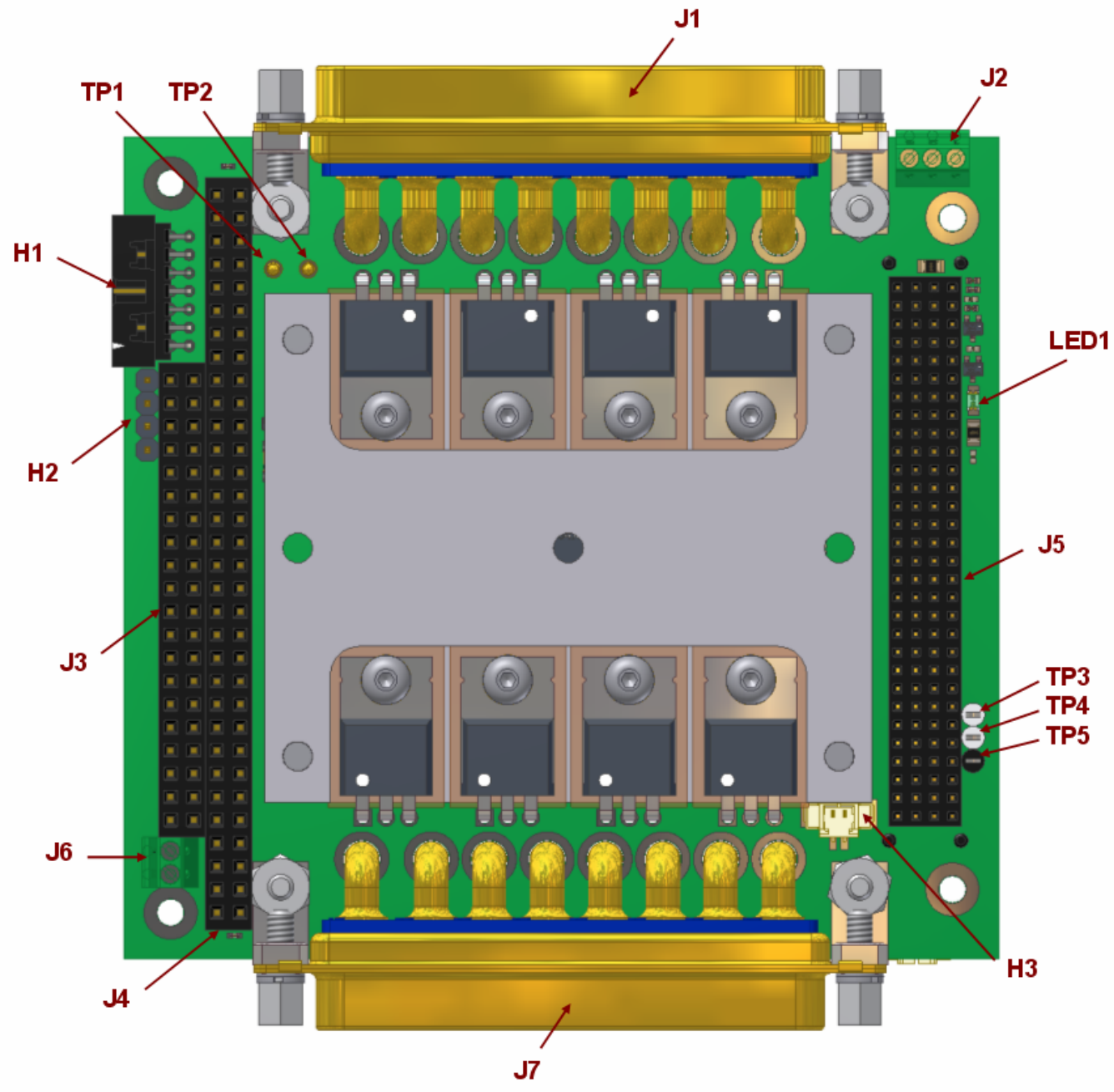


Figure 1-2. Connector Locations (Top View).

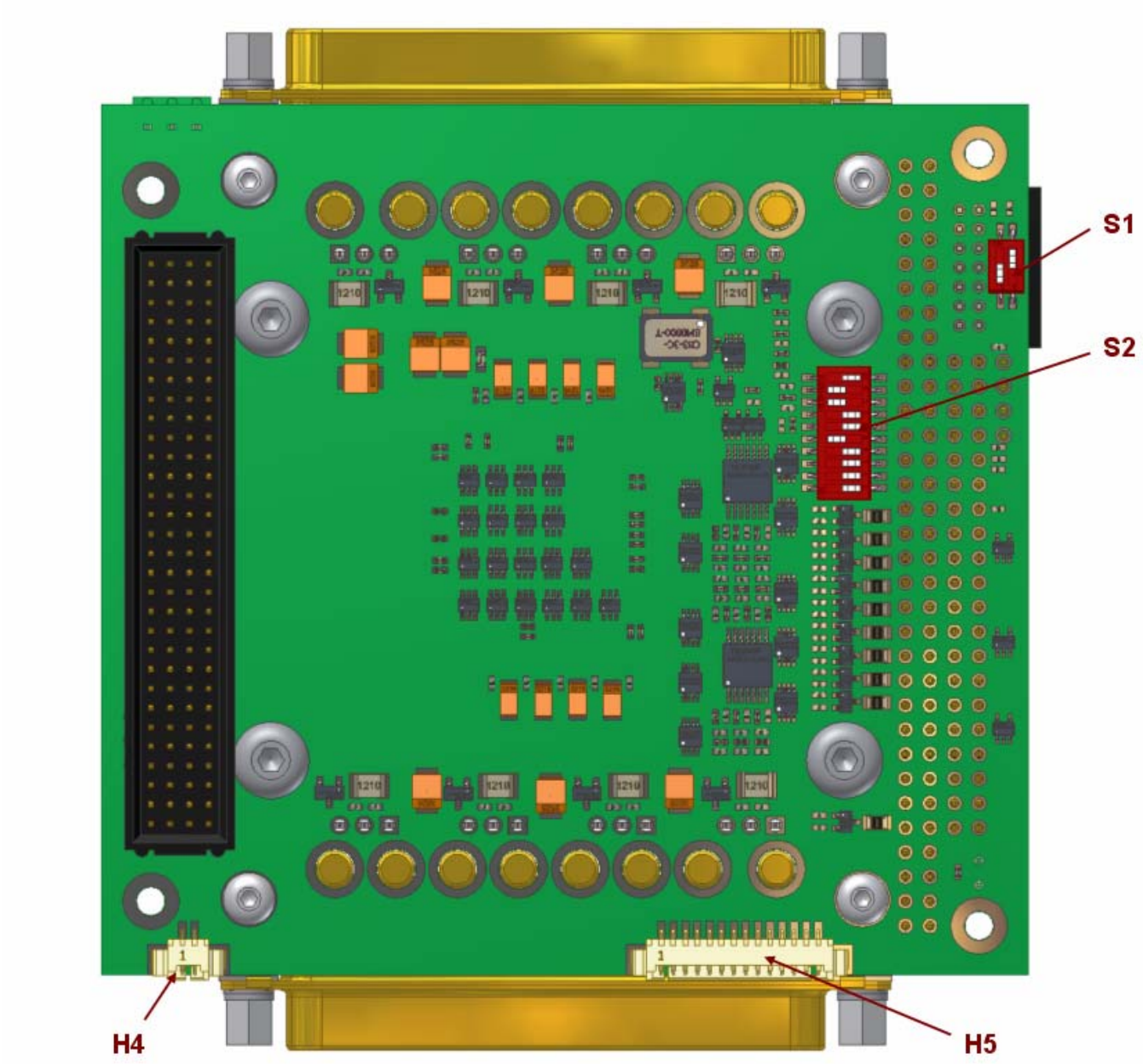


Figure 1-3. Connector Locations (Bottom View).

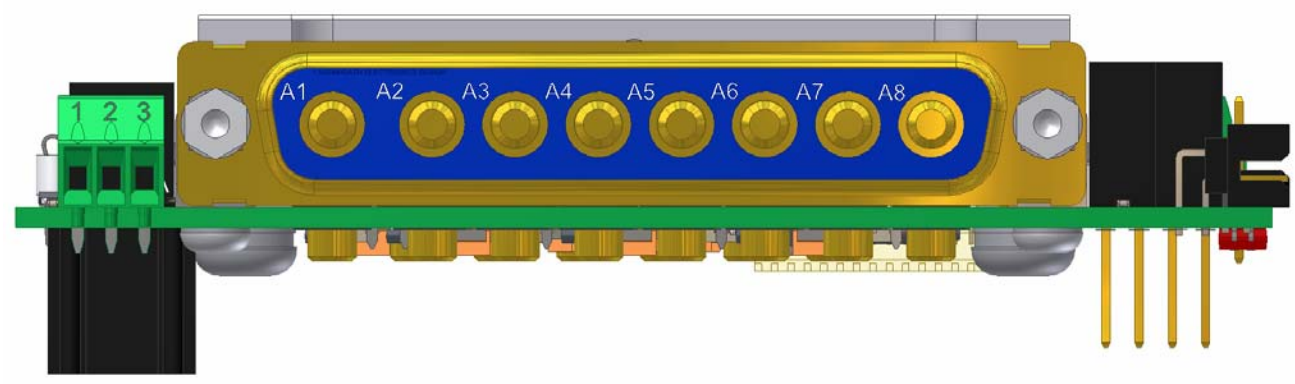


Figure 1-4. Power I/O Connector J1.

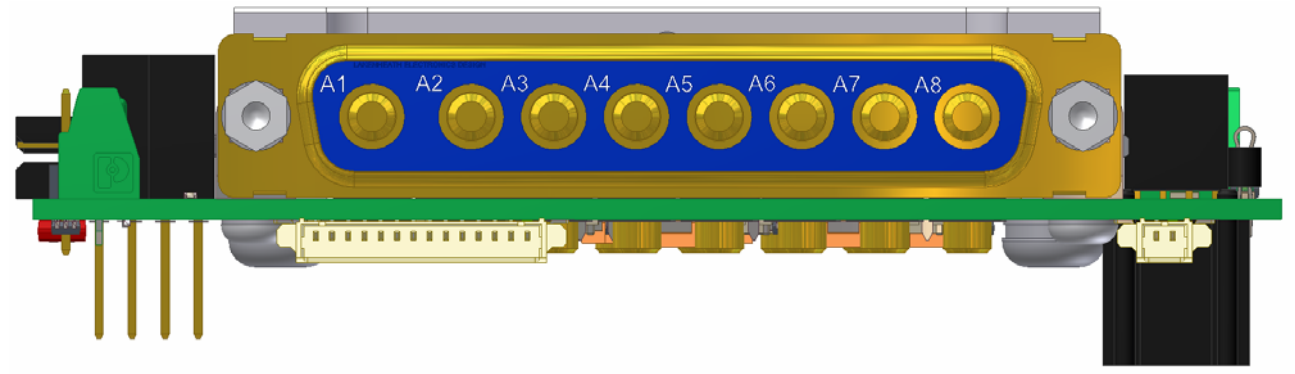


Figure 1-5. Power I/O Connector J7.

Reference	Access	Description
H1	Top	14-pin multi-function port
H2	Top	4-pin multi-function port control header
H3	Top	2-pin thermistor/heat sink interface connector
H4	Bottom	2-pin thermistor connector
H5	Bottom	LED monitor interface
J1	Top	8-pin power I/O connector, 40A contacts
J2	Top	3-pin board ground/power ground access connector
J3	Top/Bottom	40-pin PC/104 bus connector (visit www.pc104.org for spec)
J4	Top/Bottom	64-pin PC/104 bus connector (visit www.pc104.org for spec)
J5	Top/Bottom	120-pin PCI bus connector (pass-thru only)
J6	Top	Auxiliary “stand-alone” 5V power input connector
J7	Top	8-pin power I/O connector, 40A contacts
LED1	Top	Board power indicator (1Hz flasher)
S1	Bottom	Command mode selector switch
S2	Bottom	ISA I/O address switch
TP1	Top	4MHz board clock test point
TP2	Top	Decoded ISA I/O write pulse test point
TP3	Top	CPLD spare pin access
TP4	Top	CPLD spare pin access
TP5	Top	Probe ground

Table 1-1. Connector Descriptions.

H1-- Molex 87833-1420	Signal (JTAG)/(SWITCHED OR BUSSED CMD)/(RS485)	Function (JTAG)/(SWITCHED OR BUSSED CMD)/(RS485)
1	DGND/DGND/DGND	Board ground
2	EN_JTAG/NC/NC	Enable multi-function port for JTAG ops
3	GND/CMD0/CMD_SCI_EN+	JTAG ground/MOSFET 0 control/differential xcvr
4	TMS/CMD1/CMD_SCI_EN-	JTAG TMS/MOSFET 1 control/differential xcvr
5	GND/CMD2/CMD_SCI_CLK+	JTAG ground/MOSFET 2 control/differential xcvr
6	TCK/CMD3/CMD_SCI_CLK-	JTAG TCK/MOSFET 3 control/differential xcvr
7	DGND/DGND/DGND	Board ground
8	TDO/NC/NC	JTAG TCO/No connection/ No connection
9	GND/CMD4/CMD_SCI_DAT+	JTAG ground/MOSFET 4 control/differential xcvr
10	TDI/CMD5/CMD_SCI_DAT-	JTAG TDI/MOSFET 5 control/differential xcvr
11	GND/CMD6/CMD_SCI_CB+	JTAG ground/MOSFET 6 control/differential xcvr
12	NC/CMD7/CMD_SCI_CB-	No connection/MOSFET 7 control/differential xcvr
13	GND/CMDEN/NC	JTAG ground/MOSFET enable/no connection
14	NC/CMDCK/NC	no connection /MOSFET strobe/no connection

Mate: Molex 51110-1451

Table 1-2. H1 Connector Details.

H2-- Molex 90120-0764	Signal	Function
1	EN_JTAG	JTAG enabled when jumpered to H2-2. Leave open for other multi-function port uses.
2	+3P3VD	3.3 VDC
3	EN_DISC_CMD_n	Toggle switch or bussed commands enabled when jumpered to H2-4. Leave open for ISA, RS485 or push-button commands.
4	DGND	Board ground

Mate: Jumper per instructions

Table 1-3. H2 Connector Details.

H3-- Molex 53398-0271	Signal	Function
1	TRES0	Thermistor lead.
2	TRES1	Thermistor lead.

Mate: Molex 51021-0200

Table 1-4. H3 Connector Details.

H4-- Molex 53261-0271	Signal	Function
1	TRES0	Thermistor lead.
2	TRES1	Thermistor lead.

Mate: Molex 51021-0200

Table 1-5. H4 Connector Details.

H5-- Molex 53261-1471	Signal	Function (See Appendix A for suggested wiring)
1	LED_K_CMD0	Tie to external LED cathode to monitor MOSFET 0 cmd.
2	LED_K_CMD1	Tie to external LED cathode to monitor MOSFET 1 cmd.
3	LED_K_CMD2	Tie to external LED cathode to monitor MOSFET 2 cmd.
4	LED_K_CMD3	Tie to external LED cathode to monitor MOSFET 3 cmd.
5	LED_K_CMD4	Tie to external LED cathode to monitor MOSFET 4 cmd.
6	LED_K_CMD5	Tie to external LED cathode to monitor MOSFET 5 cmd.
7	LED_K_CMD6	Tie to external LED cathode to monitor MOSFET 6 cmd.
8	LED_K_CMD7	Tie to external LED cathode to monitor MOSFET 7 cmd.
9	LED_K_CMDEN	Tie to external LED cathode to monitor MOSFET latch enable.
10	LED_K_CMDCK	Tie to external LED cathode to monitor MOSFET latch strobe.
11	DGND	Board ground.
12	LED_TEST	LED test. Switch to ground to test LEDs.
13	DGND	Board ground.
14	+5VDC	Voltage source for external LEDs.

Mate: Molex 51021-1400

Table 1-6. H5 Connector Details.

J1-- Conec 5008W8PXX99N20X	Signal	Function
A1	OUT_0	Channel 0 switched power output.
A2	IN_0	Channel 0 power input.
A3	OUT_1	Channel 1 switched power output.
A4	IN_1	Channel 1 power input.
A5	OUT_2	Channel 2 switched power output.
A6	IN_2	Channel 2 power input.
A7	OUT_3	Channel 3 switched power output.
A8	IN_3	Channel 3 power input.

Mate: Conec 5008W8SXX99A10X

Table 1-7. J1 Connector Details.

J2-- Phoenix Contact 1725669	Signal	Function
1	DGND	Board ground.
2	PGND	Power ground. (reference for opto-isolator)
3	PGND	Power ground. (reference for opto-isolator)

Mate: Discrete wire screw termination.

Table 1-8. J2 Connector Details.

J6-- Phoenix Contact 1725656	Signal	Function
1	+5VDC	Input power for “stand-alone” configuration.
2	DGND	Board ground.

Mate: Discrete wire screw termination.

Table 1-9. J6 Connector Details.

J7-- Conec 5008W8PXX99N20X	Signal	Function
A1	OUT_4	Channel 4 switched power output.
A2	IN_4	Channel 4 power input.
A3	OUT_5	Channel 5 switched power output.
A4	IN_5	Channel 5 power input.
A5	OUT_6	Channel 6 switched power output.
A6	IN_6	Channel 6 power input.
A7	OUT_7	Channel 7 switched power output.
A8	IN_7	Channel 7 power input.

Mate: Conec 5008W8SXX99A10X

Table 1-10. J7 Connector Details.

2.0. OPERATION

2.1. ISA Bus.

With the PB8000 installed on a PC/104 stack, the ISA bus provides a convenient means for operating the MOSFET power channels as well as operating other functions such as the digital temperature sensor. Please see Appendix B for details concerning ISA bus operation.

2.2. RS485.

The multi-function port (H1) provides a means to communicate with the PB8000 in a half-duplex, differential bus transceiver scheme. It is assumed that the user employs the PB8000 in a "stand-alone" configuration and must therefore provide power to operate through the auxiliary power connector J6. Please see Appendix C for details concerning RS485 operation.

2.3. Toggle-Switch/8-Bit Bus.

For toggle-switch operation of the MOSFET power channels, it is assumed that the user employs the PB8000 in a "stand-alone" configuration. In this case, the board is not installed on a PC/104 stack and must therefore obtain it's power to operate from the auxiliary power connector J6. Please see Appendix D for details concerning toggle-switch operation.

2.4. Push-Button.

As with toggle-switch operation, push-button operation of the MOSFET power channels assumes that the user employs the PB8000 in a "stand-alone" configuration. Again, the board is not installed on a PC/104 stack and must therefore obtain it's power to operate from the auxiliary power connector J6. Please see Appendix E for details concerning push-button operation.

3.0. SPECIFICATIONS

3.1. Power Connector J1 and J7 Ratings.

Voltage Input Range (each channel):	18V – 36V DC
Maximum Input Current (each channel):	20A*

***NOTE: AN ADEQUATE HEAT SINK MUST BE USED AT THESE INPUT POWER LEVELS!**

3.2. Temperature Ratings.

Operating Ambient Temperature Range:	-40C to +70C
Storage Temperature Range:	-40C to +125C

3.3. Dimensions.

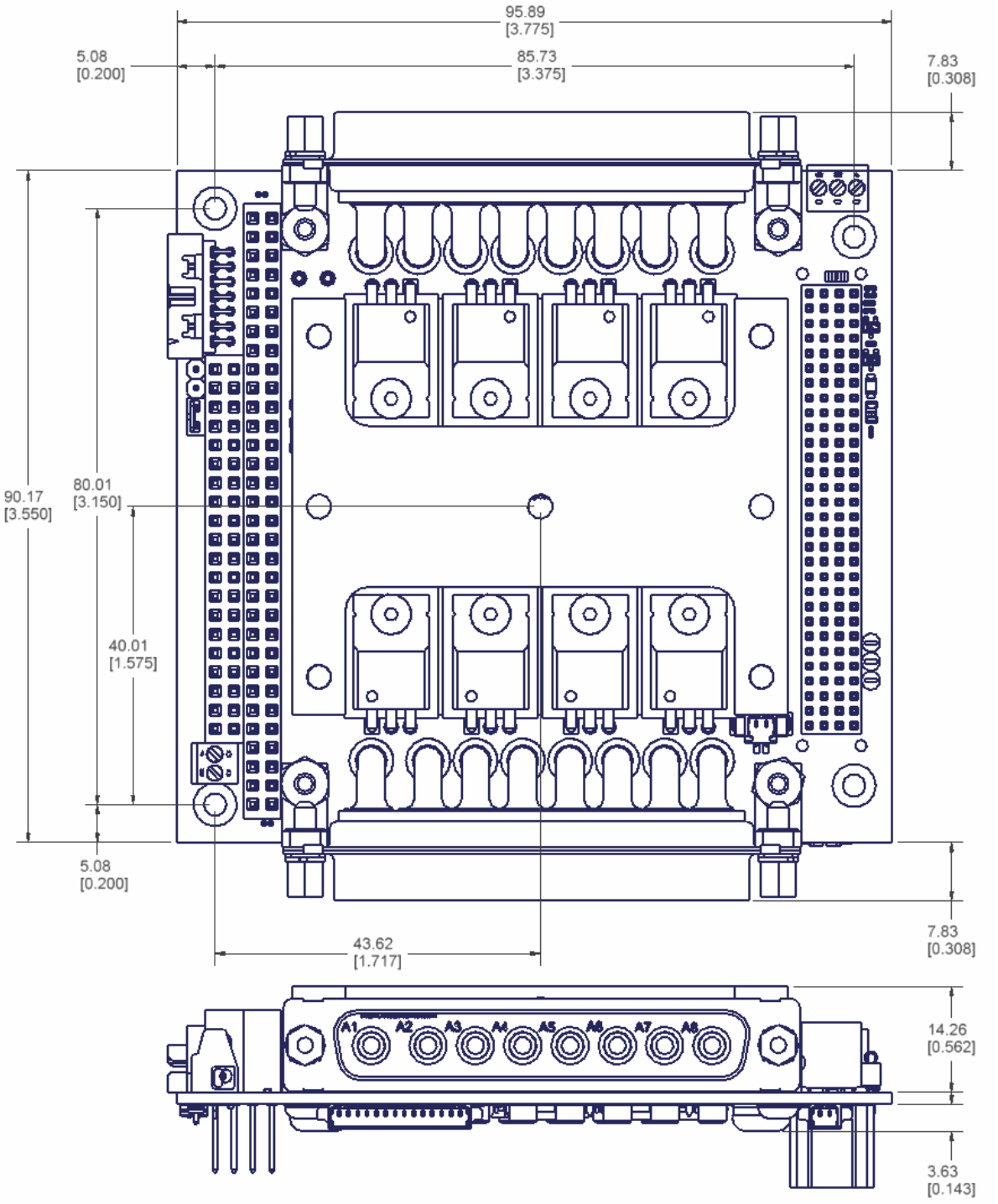


Figure 3-1. Board Dimensions.

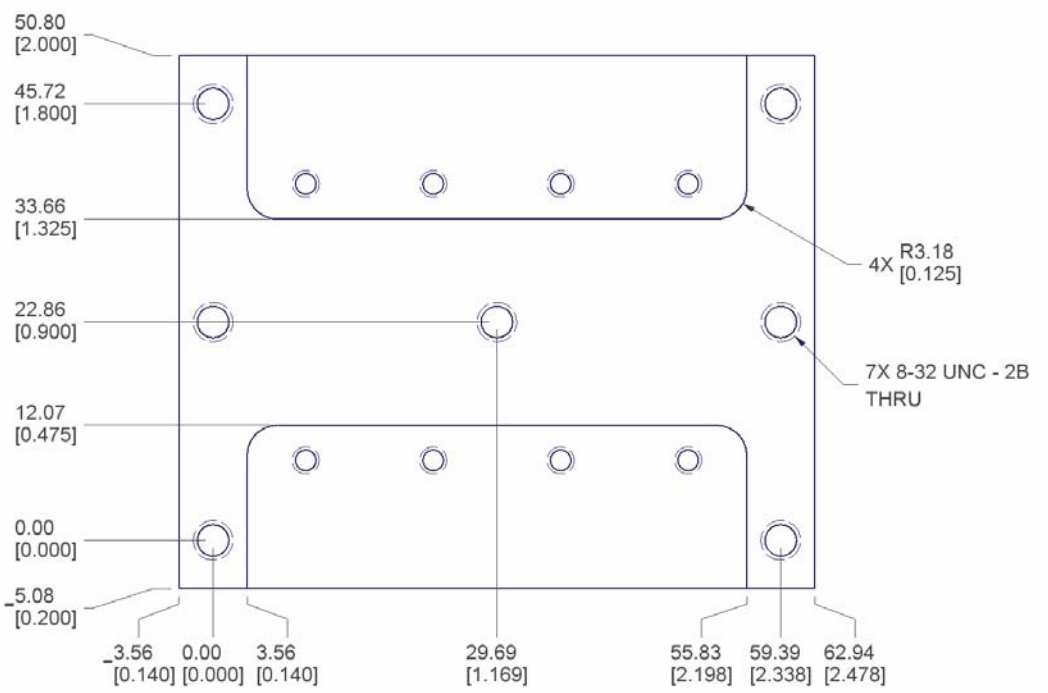


Figure 3-2. Heat Spreader Dimensions.

4.0. STRUCTURAL HEAT SINK

4.1. Conduction Cooled Chassis. As an option, the PB8000 can be configured for mounting in an aluminum dual-height fluted ring (part number LED-MP-2302). A single-height fluted ring and structural heat sink (part number LED-MP-2204) has been designed to mount to the PB8000's heat spreader in order to provide a conduction-cooled path to ambient. The single-height ring has mounting bosses to accommodate an additional PC/104 or PC/104 *Plus* board. This arrangement is shown in Figure 4-1.

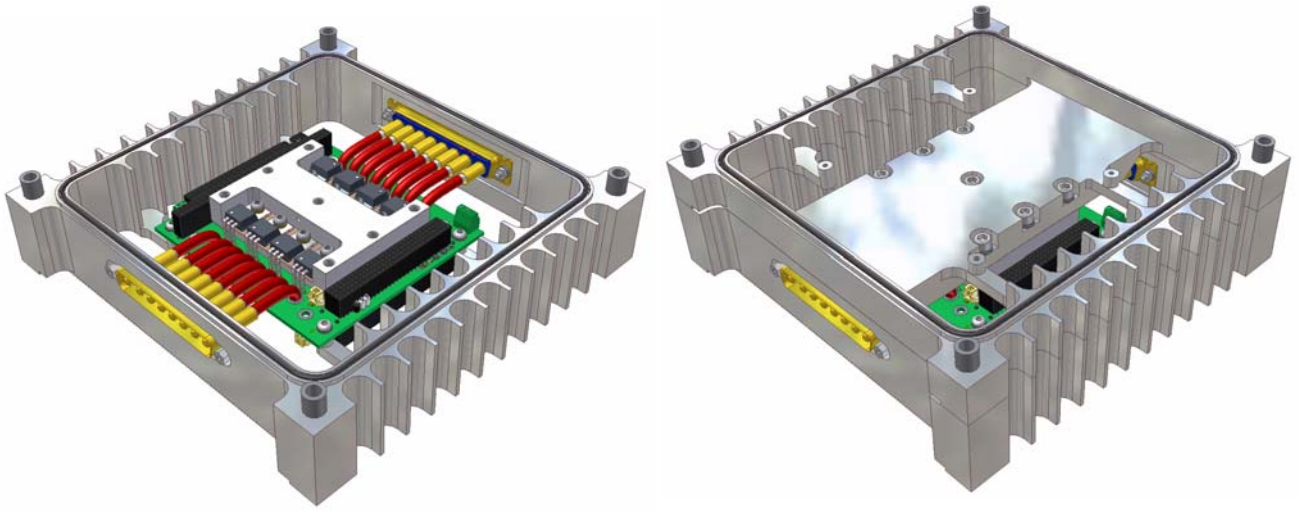


Figure 4-1. Conduction-Cooled Chassis.

When combined with a base plate, power supply and CPU, a complete embedded solution can be realized such as that show in Figure 4-2. Please contact Lakenheath Electronics Design for assistance.

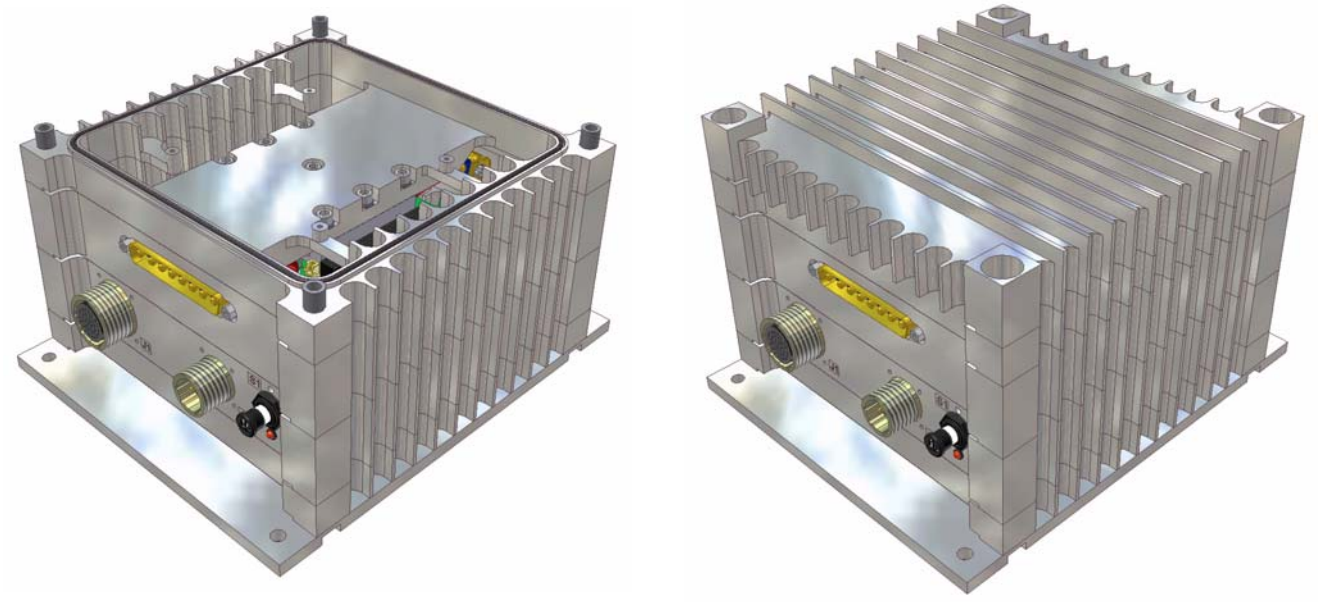


Figure 4-2. Embedded Solution.

APPENDIX A

LED MONITOR SCHEMATIC.

Figure A-1 is a schematic of suggested wiring for external LED monitors. Each LED circuit is driven by an MMST2222A-7-F NPN transistor with a 140 ohm current limiting resistor.

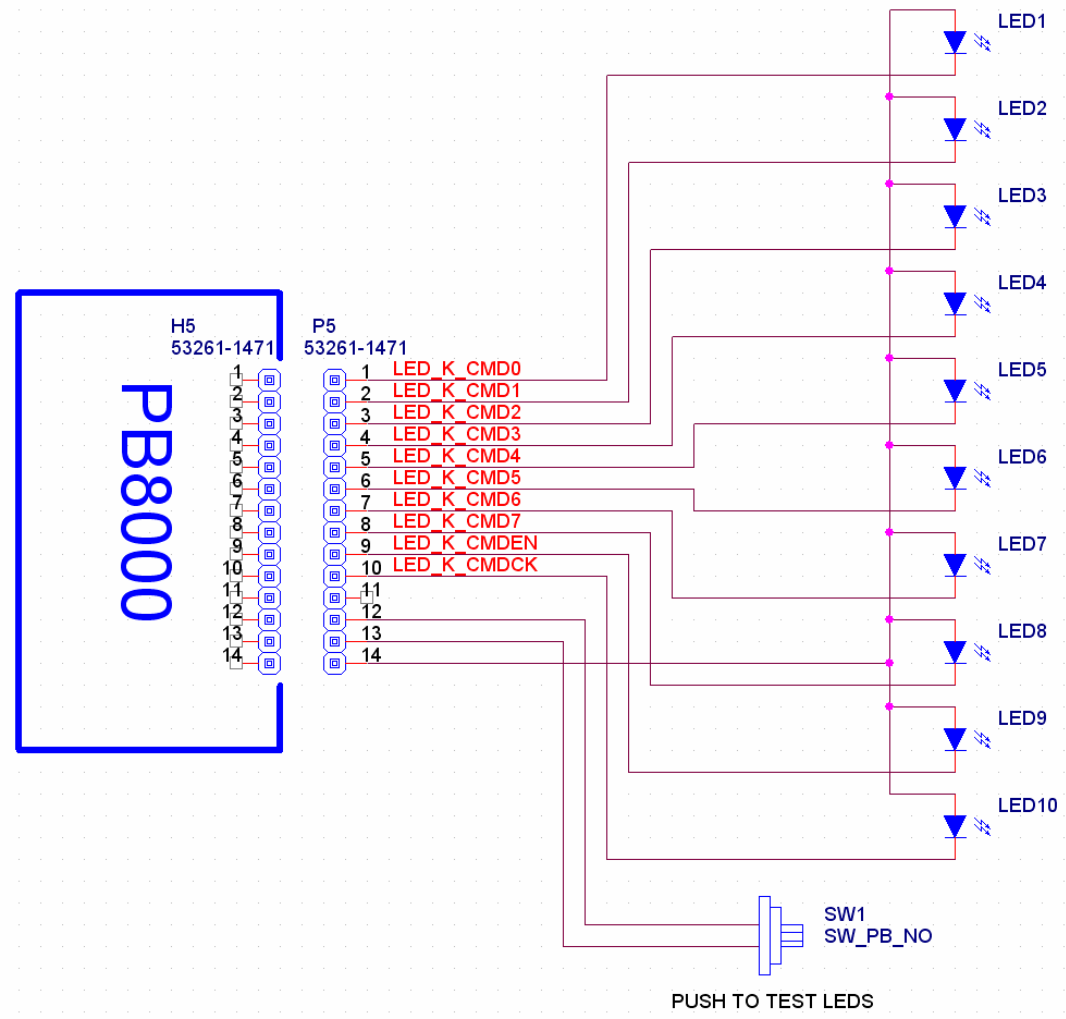


Figure A-1. LED Monitor Schematic.

APPENDIX B

ISA BUS OPERATION

B.1. Setup.

B.1.1 Verify all jumpers have been removed from header H2.

B.1.2 For ISA Bus operation, DIP switch S2 must be configured for the system reset pulse (provided by the PC/104 stack's CPU) by setting DIP switch S2-10 to **OFF** as shown in Figure B-1. DIP switch S2 is shown configured for the default I/O address 320h in accordance with Table B-1.

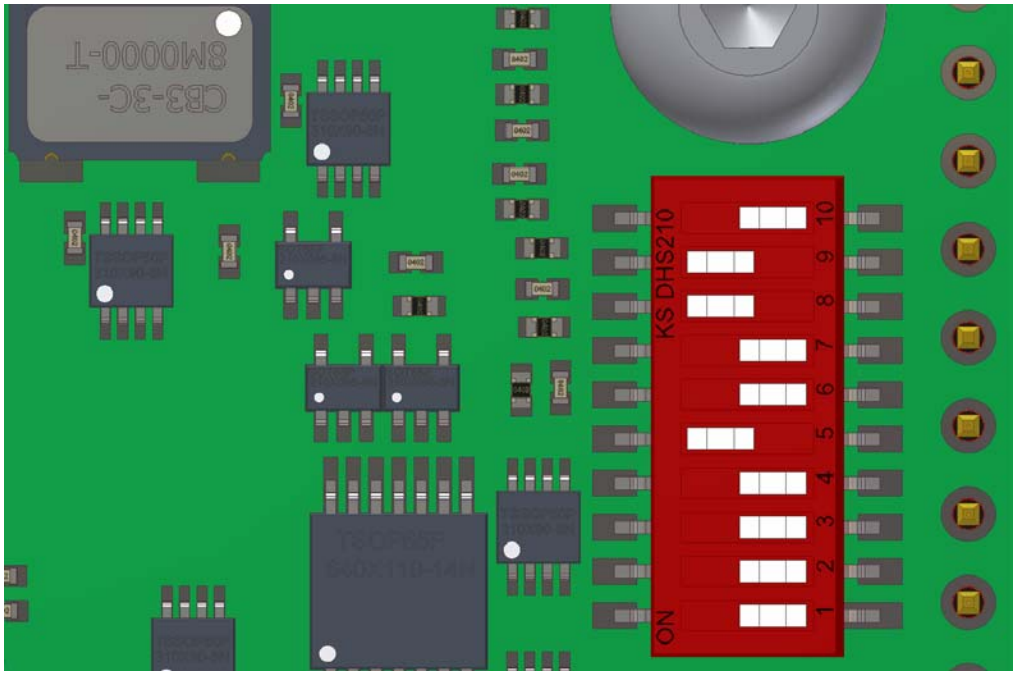


Figure B-1. Switch S2 System Reset Pulse Setting.

Switch S2-	9	8	7	6	5	4	3	2	1
Value	1	1	0	0	1	0	0	0	0

Table B-1. I/O Address 320h.

B.1.3 Verify the CPLD's DRIVER MUX is set up to select ISA Bus commands by setting DIP switch S1-1 to **OFF** and DIP switch S1-2 to **ON**. See Figure B-2.

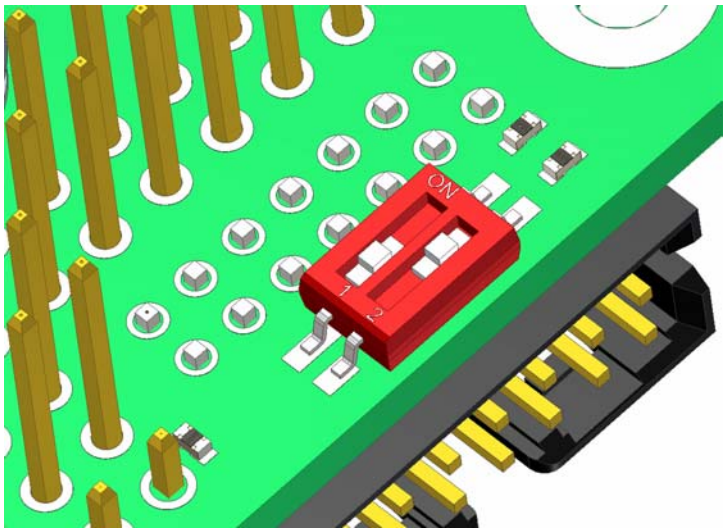


Figure B-2. Switch S1 Configuration for ISA Bus Ops.

B.2. Board Initialization.

B.2.1 The PB8000 uses the system reset to initialize registers internal to the onboard CPLD. For reliable firmware uploads to the PB8000's CPLD, the onboard clock oscillator is disabled on system power-up and must therefore be commanded on for certain commands to function. The user has a choice of enabling the onboard clock oscillator during system startup and leaving it enabled, or the user can enable the clock for those commands that require a clock and then disable the clock upon command completion. Table B-2 lists the commands for enabling and disabling the onboard clock oscillator.

Table B-2. Command Set: Clock Oscillator Commands.

Command Function	Enable Command	Disable Command	Default State
Onboard Clock Oscillator	2700h	2600h	Disabled

B.2.2 The onboard digital temperature sensor has a configuration register as well as under-temperature and over-temperature set points that require initializing. Please see the Digital Temperature Sensor section for further information.

B.3. MOSFET Power Channel Commands.

B.3.1 The MOSFET power channels are operated in a double-buffered command scheme. A 16-bit command with a base value of 2000h is built to switch on or off the desired power channels in accordance with Table B-3. An ISA write loads this command into the MOSFET Driver Command Latch. A subsequent ISA write with command 2100h transfers the contents of the MOSFET Driver Command Latch into the MOSFET Driver Output Latch thereby updating the states of the MOSFET power

channels. For example, to switch on power channels 1, 4 and 6 (while leaving the remaining channels off), the low bytes of the enable commands 2002h, 2010h and 2040h are added together to obtain 2052h. Two ISA write commands, 2052h and 2100h, are sent to achieve the desired result. If external LEDs are connected to H5, then the corresponding LEDs for channels 1, 4 and 6 will illuminate while the remaining LEDs will be off. *Note: The onboard clock oscillator must be enabled for the LEDs to operate. If desired, the clock oscillator may be disabled after the MOSFET power channel commands have been sent without disturbing the states of the LEDs.* Below is a sample command sequence that captures what has been described above:

```
w_isa(2700, 0320) // Enable clock oscillator.
w_isa(2052, 0320) // Load command into MOSFET Driver Command Latch.
w_isa(2100, 0320) // Latch command into MOSFET Driver Output Latch.
w_isa(2600, 0320) // Disable clock oscillator.
```

Table B-3. Command Set: MOSFET Driver Commands.

Command Function	Enable Command	Disable Command	Default State
MOSFET Power Channel 0	2001h	2000h	Disabled
MOSFET Power Channel 1	2002h	2000h	Disabled
MOSFET Power Channel 2	2004h	2000h	Disabled
MOSFET Power Channel 3	2008h	2000h	Disabled
MOSFET Power Channel 4	2010h	2000h	Disabled
MOSFET Power Channel 5	2020h	2000h	Disabled
MOSFET Power Channel 6	2040h	2000h	Disabled
MOSFET Power Channel 7	2080h	2000h	Disabled

Command Function	Hex Command Word
Load MOSFET Driver Output Latch.	2100h
Select the MOSFET Driver Status Buffer for an ISA read.	22e0h

B.4. MOSFET Power Channel Status.

B.4.1 The status of the MOSFET power channels can be read by first sending an ISA write of 22e0h. *Note: This command does not require an enabled clock oscillator.* This command prepares the MOSFET Driver Status Buffer to make its contents available to the ISA bus. By following the ISA write with an ISA read, the host computer obtains the contents of the status buffer. The low byte of the 16-bit data word contains the status whereas the high byte will have a value of zero. A possible arrangement for a MOSFET power channel control GUI is shown in Figure B-3.

Figure B-3. Suggested MOSFET Power Channel Control GUI.

B.5. Digital Temperature Sensor.

B.5.1 A Dallas Semiconductor DS1626 digital temperature sensor thermally coupled to the power MOSFETs' heat spreader can be used to monitor the heat spreader's temperature. The DS1626 includes on-chip EEPROM for storing programmable over-temperature and under-temperature thresholds. The DS1626's status lines can be polled to check if these thresholds have been exceeded. A slight drawback with the DS1626 is that the device expects serial commands to be sent with the LSB first. The device also transmits serial data with the LSB first. However, the PB8000's onboard serial transceiver has been designed from an MSB first perspective. Once this is understood, the commands and data can be manipulated to operate the DS1626.

B.5.2 The DS1626 has an eight-bit configuration register with four bits of non-volatile EEPROM. The configuration register recalls the last values written to these bits on power-up. Table B-4 below is reproduced from the DS1626 data sheet. The following command sequence will write a zero to the 1SHOT bit, and ones to the CPU, R0 and R1 bits. Please see the DS1626 data sheet for further details.

```
w_isa(2700, 0320) // Enable clock oscillator.
w_isa(2500, 0320) // Enable CPLD's Byte 1 Reg to accept ISA data.
w_isa(2800, 0320) // Load CPLD's Byte 0 Reg with byte 00h.
w_isa(2970, 0320) // Load CPLD's Byte 1 Reg with byte 70h.
w_isa(2a30, 0320) // Load CPLD's Byte 2 Reg with byte 30h.
w_isa(2b02, 0320) // Set Sync Designation Reg for sync 1.
w_isa(2cf0, 0320) // Set Serial Clock Count Reg for 16-bit data.
w_isa(2ef0, 0320) // Set Serial Data Count Reg for 16-bit data.
w_isa(2d00, 0320) // Set Polarity Reg for non-inv en & non-inv clk.
w_isa(2400, 0320) // Clear Slave Data Enable Latch.
w_isa(2f00, 0320) // Transmit data to DS1626 Cfg Reg.
w_isa(2600, 0320) // Disable clock oscillator.
```

Table B-4. DS1626 Configuration Register Bit Descriptions.

BIT NAME (USER ACCESS)	FUNCTIONAL DESCRIPTION
DONE (Read Only)	Power-up state = 1. DONE = 0. Temperature conversion is in progress. DONE = 1. Temperature conversion is complete.
THF (Read/Write)	Power-up state = 0. THF = 1. The measured temperature has reached or exceeded the value stored in the T_H register. THF will remain a 1 until it is overwritten with a 0 by the user, the power is cycled, or a Software POR command is issued.
TLF (Read/Write)	Power-up state = 0. TLF = 1. The measured temperature has equaled or dropped below the value stored in the T_L register. TLF will remain a 1 until it is overwritten with a 0 by the user, the power is cycled, or a Software POR command is issued.
NVB (Read Only)	Power-up state = 0. NVB = 1. Write to an E^2 memory cell is in progress. NVB = 0. NV memory is not busy.
R1* (Read/Write)	Power-up state = last value written to this bit. Sets conversion resolution (see Table 6). Initial state from factory = 1.
R0* (Read/Write)	Power-up state = last value written to this bit. Sets conversion resolution (see Table 6). Initial state from factory = 1.
CPU* (Read/Write)	Power-up state = last value written to this bit. CPU = 1. Stand-alone mode is disabled. CPU = 0. Stand-alone mode is enabled when RST = 0. See *CPU BIT AND STAND-ALONE THERMOSTAT OPERATION* section for more information. Initial state from factory = 0.
1SHOT* (Read/Write)	Power-up state = last value written to this bit. 1SHOT = 1: One-Shot Mode. The Start Convert T command initiates a single temperature conversion and then the device goes into a low-power standby state. 1SHOT = 0: Continuous Conversion Mode. The Start Convert T command initiates continuous temperature conversions. Initial state from factory = 0.

*NV (EEPROM)

B.5.3 The DS1626 has user-programmable over-temperature (T_H) and under-temperature (T_L) thresholds that are stored in on-chip, non-volatile EEPROM. The following command sequence will set the over-temperature threshold to +75C. Please see the DS1626 data sheet for further details.

```
w_isa(2700, 0320) // Enable clock oscillator.
w_isa(2500, 0320) // Enable CPLD's Byte 1 Reg to accept ISA data.
w_isa(2820, 0320) // Load CPLD's Byte 0 Reg with byte 20h.
w_isa(290d, 0320) // Load CPLD's Byte 1 Reg with byte 0dh.
w_isa(2a80, 0320) // Load CPLD's Byte 2 Reg with byte 80h.
w_isa(2b02, 0320) // Set Sync Designation Reg for sync 1.
w_isa(2cec, 0320) // Set Serial Clock Count Reg for 20-bit data.
w_isa(2eec, 0320) // Set Serial Data Count Reg for 20-bit data.
```

```
w_isa(2d00, 0320) // Set Polarity Reg for non-inv en & non-inv clk.
w_isa(2300, 0320) // Set Slave Data Enable Latch.
w_isa(2f00, 0320) // Transmit data to DS1626 Over-Temp Reg.
w_isa(2600, 0320) // Disable clock oscillator.
```

The following command sequence will set the under-temperature threshold to -10C. Please see the DS1626 data sheet for further details.

```
w_isa(2700, 0320) // Enable clock oscillator.
w_isa(2500, 0320) // Enable CPLD's Byte 1 Reg to accept ISA data.
w_isa(28f0, 0320) // Load CPLD's Byte 0 Reg with byte f0h.
w_isa(2906, 0320) // Load CPLD's Byte 1 Reg with byte 06h.
w_isa(2a80, 0320) // Load CPLD's Byte 2 Reg with byte 80h.
w_isa(2b02, 0320) // Set Sync Designation Reg for sync 1.
w_isa(2cec, 0320) // Set Serial Clock Count Reg for 20-bit data.
w_isa(2eec, 0320) // Set Serial Data Count Reg for 20-bit data.
w_isa(2d00, 0320) // Set Polarity Reg for non-inv en & non-inv clk.
w_isa(2300, 0320) // Set Slave Data Enable Latch.
w_isa(2f00, 0320) // Transmit data to DS1626 Under-Temp Reg.
w_isa(2600, 0320) // Disable clock oscillator.
```

B.5.4 The DS1626 over-temperature (T_H) and under-temperature (T_L) threshold registers can be read. The following command sequence will read the over-temperature threshold register:

```
w_isa(2700, 0320) // Enable clock oscillator.
w_isa(2500, 0320) // Enable CPLD's Byte 1 Reg to accept ISA data.
w_isa(2800, 0320) // Load CPLD's Byte 0 Reg with byte 00h.
w_isa(2900, 0320) // Load CPLD's Byte 1 Reg with byte 00h.
w_isa(2a85, 0320) // Load CPLD's Byte 2 Reg with byte 85h.
w_isa(2b02, 0320) // Set Sync Designation Reg for sync 1.
w_isa(2ce8, 0320) // Set Serial Clock Count Reg for 24-bit data.
w_isa(2ef8, 0320) // Set Serial Data Count Reg for 8-bit data.
w_isa(2d00, 0320) // Set Polarity Reg for non-inv en & non-inv clk.
w_isa(2300, 0320) // Set Slave Data Enable Latch.
w_isa(2f00, 0320) // Transmit data to DS1626.
w_isa(22a0, 0320) // Set Read Data Control for Auxiliary Data.
w_isa(2600, 0320) // Disable the clock oscillator.
r_isa(0320) // Perform an ISA read.
```

The following command sequence will read the under-temperature threshold register:

```
w_isa(2700, 0320) // Enable clock oscillator.
w_isa(2500, 0320) // Enable CPLD's Byte 1 Reg to accept ISA data.
w_isa(2800, 0320) // Load CPLD's Byte 0 Reg with byte 00h.
w_isa(2900, 0320) // Load CPLD's Byte 1 Reg with byte 00h.
w_isa(2a45, 0320) // Load CPLD's Byte 2 Reg with byte 45h.
w_isa(2b02, 0320) // Set Sync Designation Reg for sync 1.
w_isa(2ce8, 0320) // Set Serial Clock Count Reg for 24-bit data.
w_isa(2ef8, 0320) // Set Serial Data Count Reg for 8-bit data.
w_isa(2d00, 0320) // Set Polarity Reg for non-inv en & non-inv clk.
w_isa(2300, 0320) // Set Slave Data Enable Latch.
w_isa(2f00, 0320) // Transmit data to DS1626.
w_isa(22a0, 0320) // Set Read Data Control for Auxiliary Data.
w_isa(2600, 0320) // Disable the clock oscillator.
r_isa(0320) // Perform an ISA read.
```

B.5.5 With the DS1626 configuration register configured as indicated above, the DS1626 will operate in continuous temperature conversion mode once it receives a Start Convert T command. The following command sequence will start the DS1626 continuous temperature conversion:

```
w_isa(2700, 0320) // Enable clock oscillator.
w_isa(2500, 0320) // Enable CPLD's Byte 1 Reg to accept ISA data.
w_isa(2800, 0320) // Load CPLD's Byte 0 Reg with byte 00h.
w_isa(2900, 0320) // Load CPLD's Byte 1 Reg with byte 00h.
w_isa(2a8a, 0320) // Load CPLD's Byte 2 Reg with byte 8ah.
w_isa(2b02, 0320) // Set Sync Designation Reg for sync 1.
w_isa(2cf8, 0320) // Set Serial Clock Count Reg for 8-bit data.
w_isa(2ef8, 0320) // Set Serial Data Count Reg for 8-bit data.
w_isa(2d00, 0320) // Set Polarity Reg for non-inv en & non-inv clk.
w_isa(2400, 0320) // Clear Slave Data Enable Latch.
w_isa(2f00, 0320) // Transmit data to DS1626.
w_isa(2600, 0320) // Disable clock oscillator.
```

B.5.6 Once the DS1626 has been placed in continuous temperature conversion mode, the DS1626 temperature can be read with the following command sequence:

```
w_isa(2700, 0320) // Enable clock oscillator.
w_isa(2500, 0320) // Enable CPLD's Byte 1 Reg to accept ISA data.
w_isa(2800, 0320) // Load CPLD's Byte 0 Reg with byte 00h.
w_isa(2900, 0320) // Load CPLD's Byte 1 Reg with byte 00h.
w_isa(2a55, 0320) // Load CPLD's Byte 2 Reg with byte 55h.
w_isa(2b02, 0320) // Set Sync Designation Reg for sync 1.
w_isa(2ce8, 0320) // Set Serial Clock Count Reg for 24-bit data.
w_isa(2ef8, 0320) // Set Serial Data Count Reg for 8-bit data.
w_isa(2d00, 0320) // Set Polarity Reg for non-inv en & non-inv clk.
w_isa(2300, 0320) // Set Slave Data Enable Latch.
w_isa(2f00, 0320) // Transmit data to DS1626.
w_isa(22a0, 0320) // Set Read Data Control for Auxiliary Data.
w_isa(2600, 0320) // Disable the clock oscillator.
r_isa(0320) // Perform an ISA read.
```

The returned data is a 16-bit word that must be manipulated for interpretation. Figure B-4 is graphic of LabVIEW® code that shows one way the returned data can be handled. The data handling for data read from the over-temperature and under-temperature threshold registers is the same.

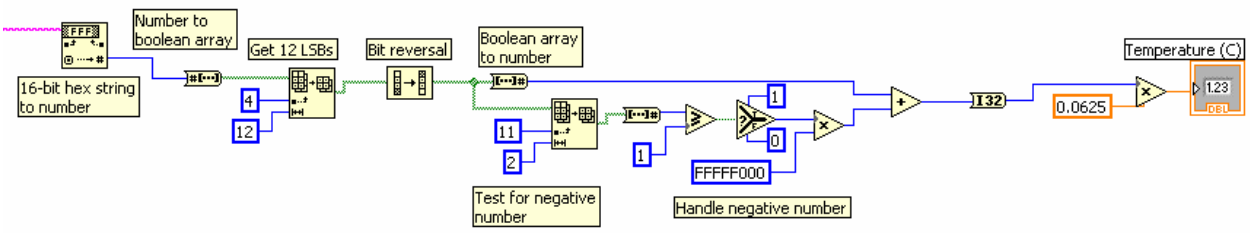


Figure B-4. Suggested DS1626 Threshold Register Data Handling.

A possible arrangement for a digital temperature sensor control GUI is shown in Figure B-5.

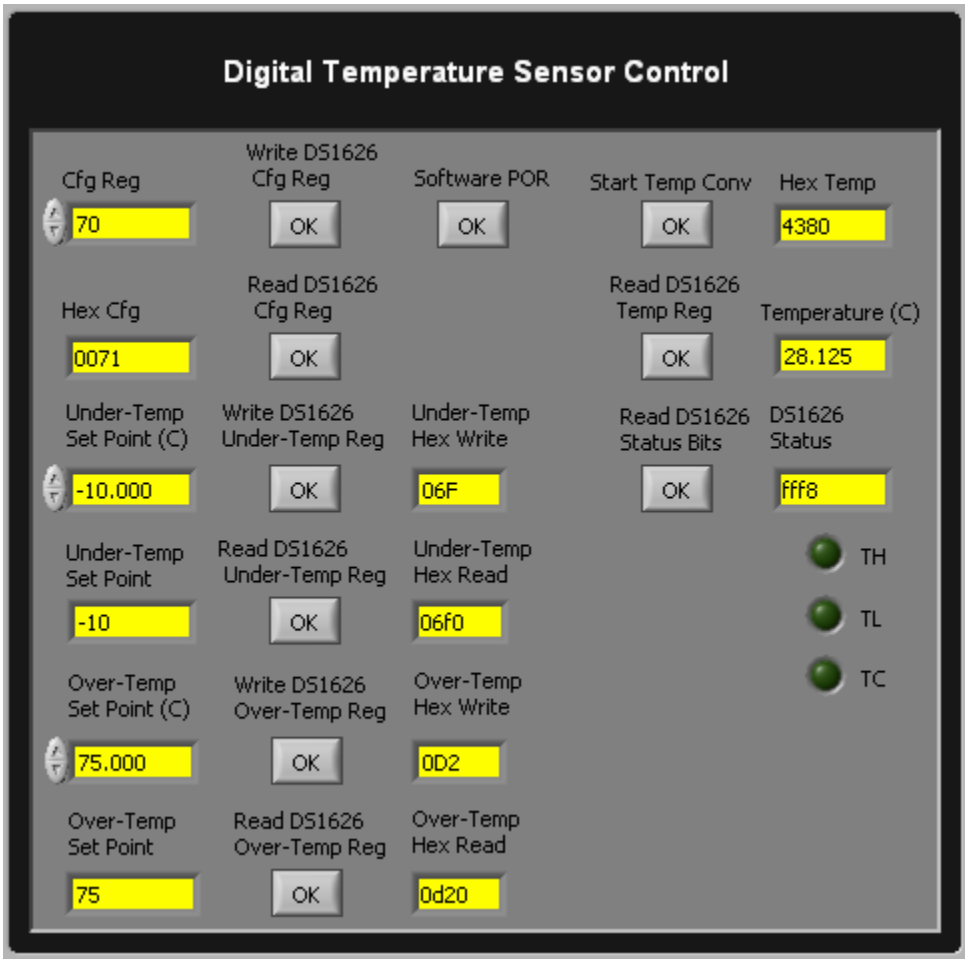


Figure B-5. Suggested DS1626 Digital Temperature Sensor Control GUI.

B.5.7 The following command sequence will read the three DS1626 status bits:

```
w_isa(22c0, 0320) // Set Read Data Control for External Data.
r_isa(0320) // Perform an ISA read.
```

The returned data is a 16-bit word that can be handled with the suggested LabVIEW® code shown in Figure B-6:

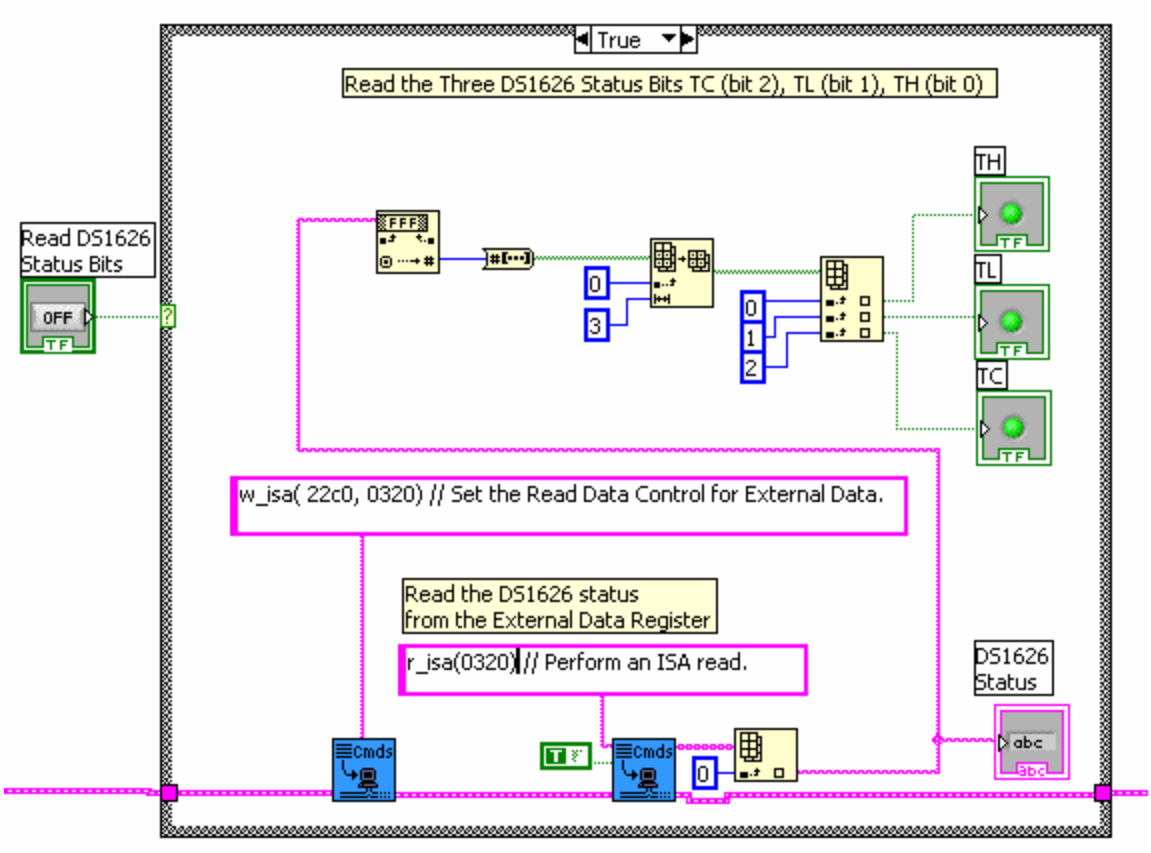


Figure B-6. Suggested DS1626 Status Register Data Handling.

APPENDIX C

RS-485 OPERATION

Figure C-1 diagrams the configuration of the PB8000 wiring in an RS485 communications scheme. Three transceivers consisting of an active high enable (EN), a serial clock (CLK) and data (DAT) are used for the data bus. Data consists of 16-bit words with the MSB transmitted first. A fourth transceiver serves as a control bus transceiver. On system power-up, the PB8000 defaults to receive commands from the host computer.

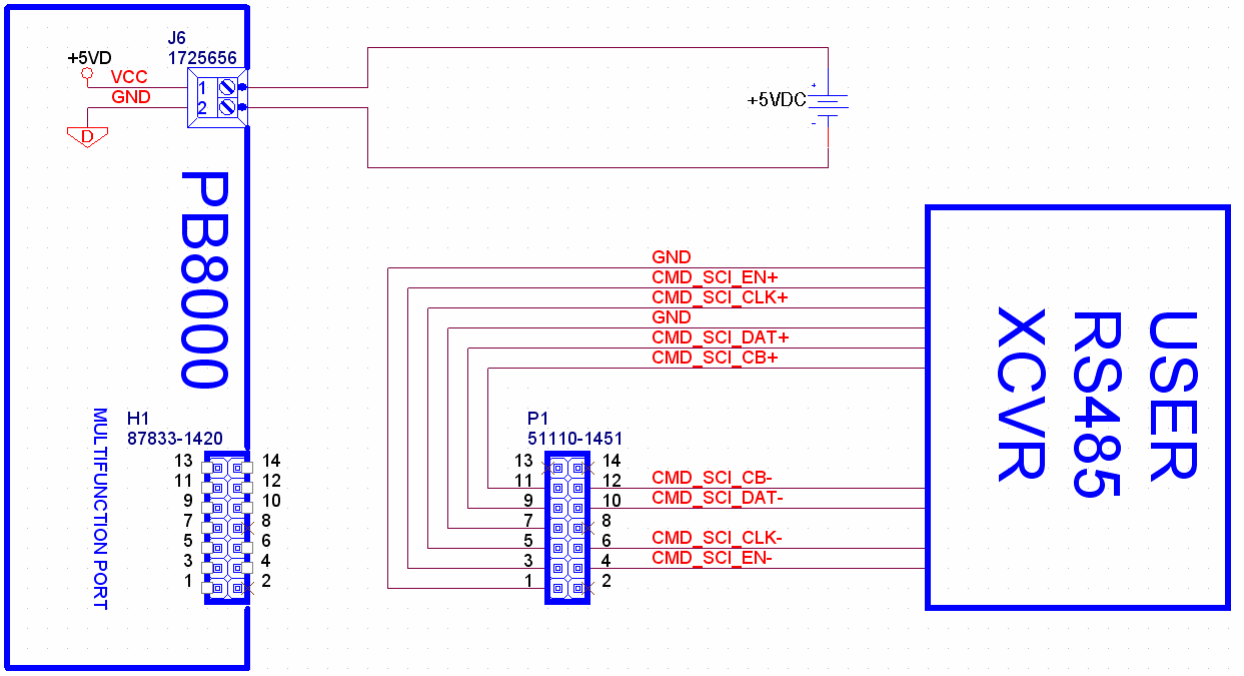


Figure C-1. RS485 Configuration Diagram.

C.1. The timing diagram for a serial transaction from the host computer to the PB8000 is illustrated in Figure C-2. The protocol consists of lowering the command control bus line (CMD_CB) in order to clear the PB8000's Control Bus XCVR Latch thus enabling the PB8000's command receiver. The CMD_CB control line's active-low status can be as short as half a CMD_CLK clock cycle or, if it simplifies programming, this signal can remain low for as long as it takes to send a sequence of 16-bit command words. At the same time CMD_CB is lowered, the word strobe CMD_EN is raised. The word strobe remains high for the duration of the 16 synchronizing clock pulses (CMD_CLK) that follow. Data (CMD_DAT) is clocked in on the rising edges of CMD_CLK. See Appendix B for the command set.

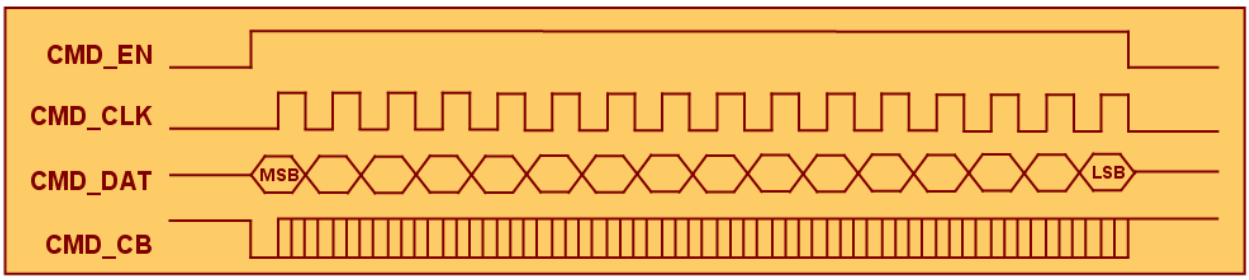


Figure C-2. RS485 Serial Transaction: Host to PB8000.

C.2. The timing diagram for a serial transaction from the PB8000 to the host computer is illustrated in Figure C-3. To simplify debugging, the protocol is identical to that of transmitting data from the host computer to the PB8000.

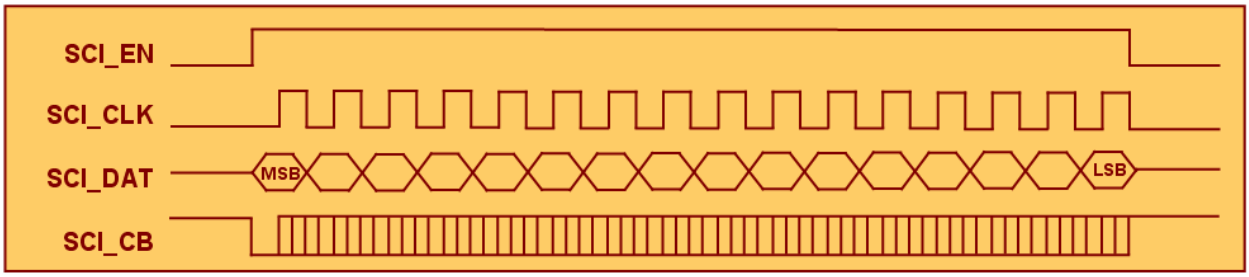


Figure C-3. RS485 Serial Transaction: PB8000 to Host.

C.3. Verify all jumpers have been removed from header H2 to enable the multifunction port H1 to accept RS485 commands.

C.4. For stand-alone operation, DIP switch S2 must be configured for onboard reset pulse by setting DIP switch S2-10 to **ON** as shown in Figure C-4.

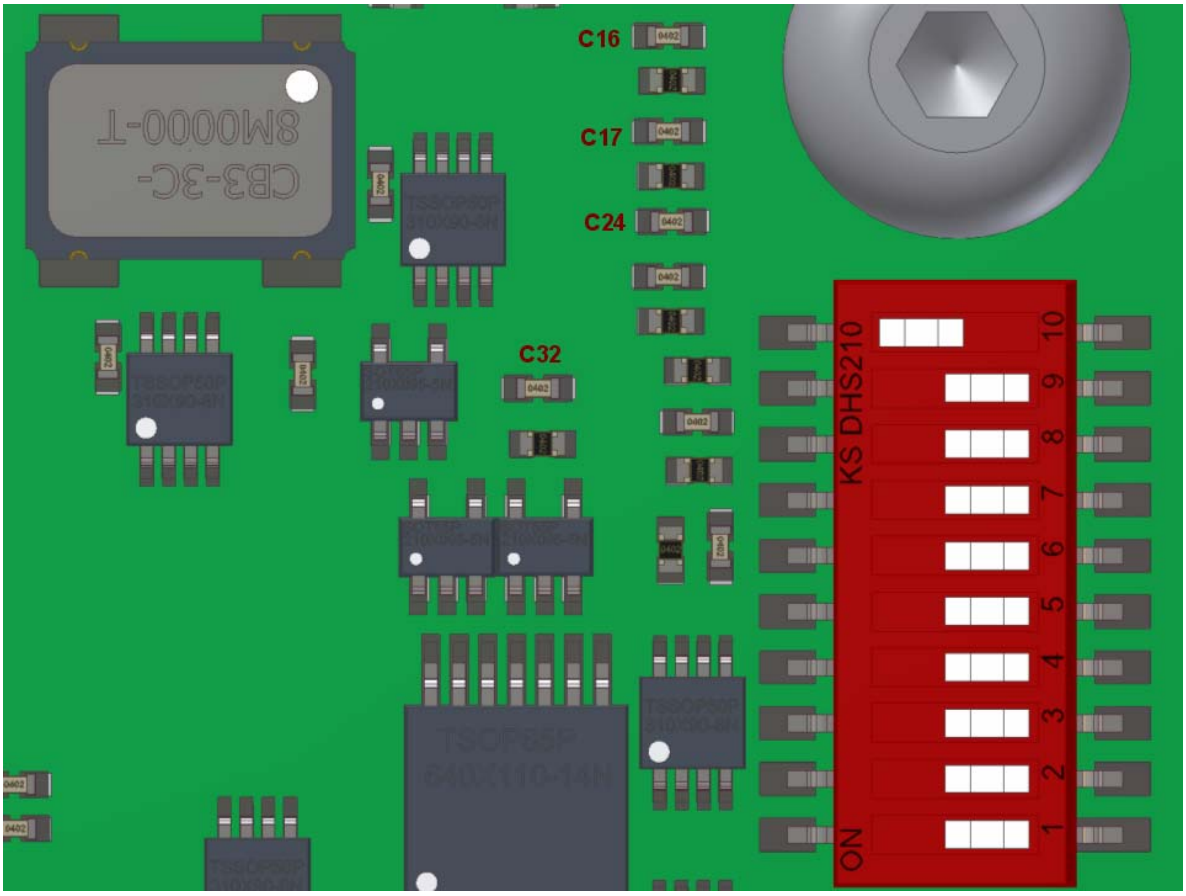


Figure C-4. Switch S2 Onboard Reset Pulse Setting.

C.5. Verify the CPLD's DRIVER MUX is set up to select RS485 commands by setting DIP switch S1-1 to **OFF** and DIP switch S1-2 to **ON**. See Figure C-5.

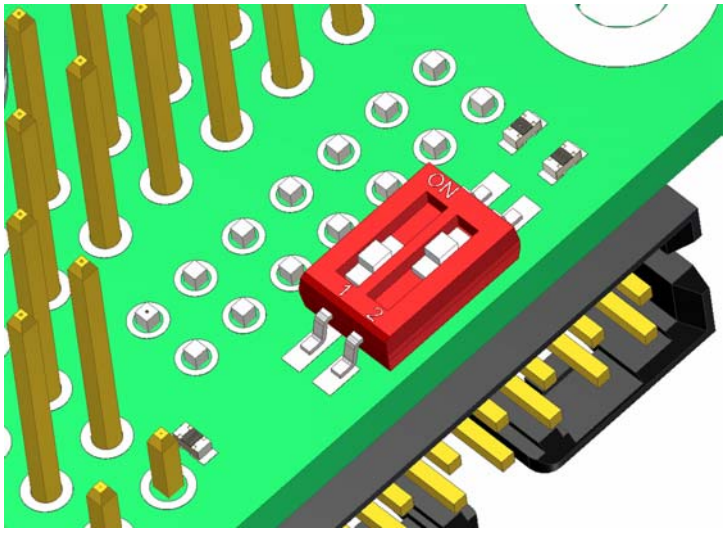


Figure C-5. S1 Configuration for RS485 Ops.

C.6. Verify the command cable is connected between the external RS485 transceiver and multifunction port H1.

C.7. Verify that a +5VDC supply cable has been attached to auxiliary power connector J6.

C.8. Verify that cables have been attached to connectors J1 and/or J7 to supply power to be switched by the MOSFET power channels.

C.9. Switch **ON** power to the auxiliary power connector J6.

C.10. Switch **ON** the input power to the MOSFET power channels.

C.11. If external MOSFET monitoring LEDs are used, verify that these are **OFF**.

C.12. Communicate with the PB8000 using commands from the command set in Appendix B.

C.13. When finished with operating the PB8000, switch **OFF** the input power to the MOSFETs.

C.14. Switch **OFF** power to the auxiliary power connector J6.

APPENDIX D

TOGGLE-SWITCH/8-BIT BUS OPERATION

Figure D-1 is a schematic of a possible arrangement for operating the MOSFET power channels using single pole, double throw (SPDT) toggle switches. Note: As an alternative, the toggle-switches could be replaced with an 8-bit bus plus an enable line (CMDEN) and a strobe line (CMDCK). For either situation, the sequence outlined below illustrates how to control MOSFET power channel 0.

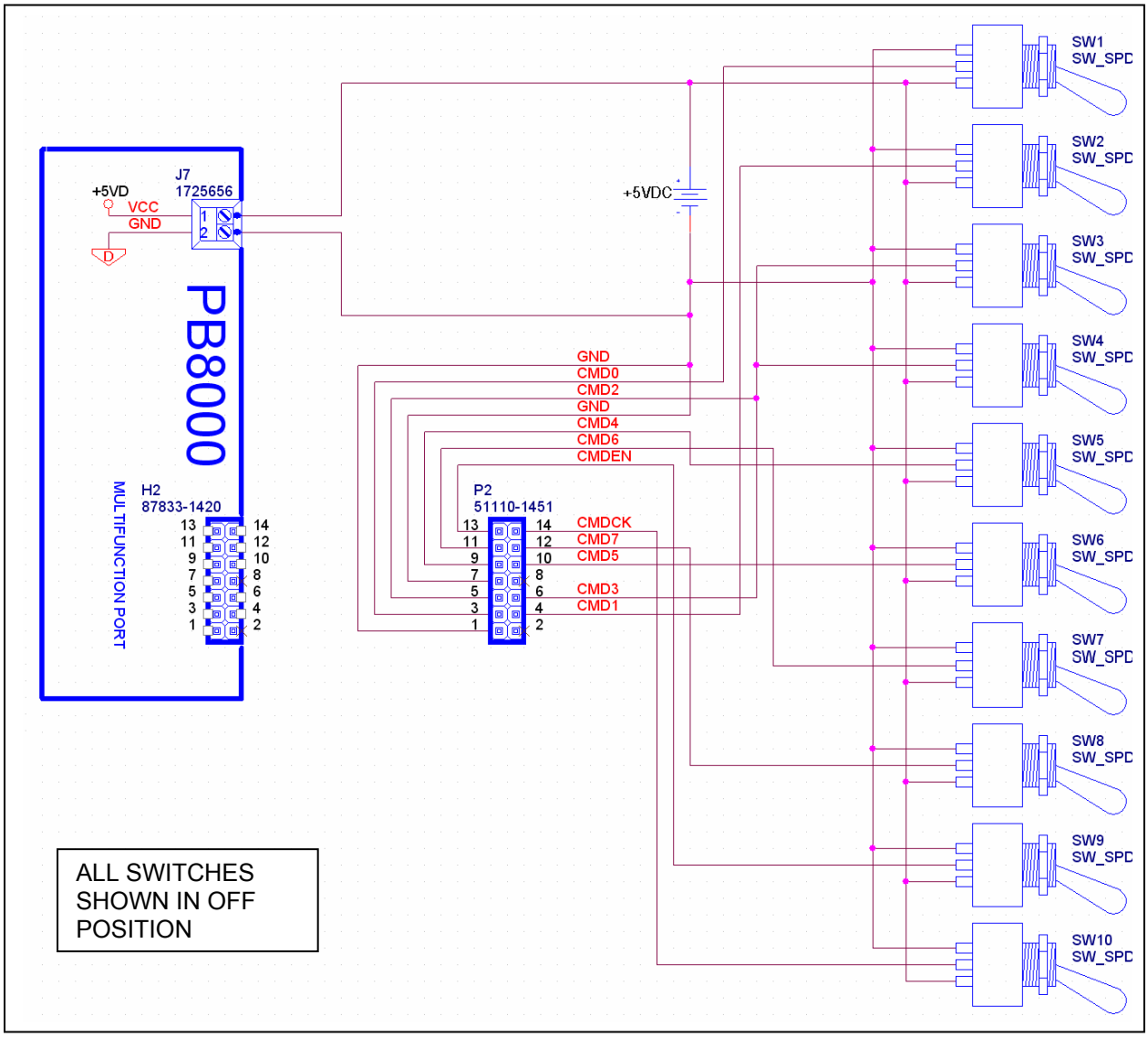


Figure D-1. Toggle-Switch Schematic.

D.1. Configure DIP switch S2 for onboard reset pulse by setting DIP switch S2-10 to **ON** as shown in Figure D-2.

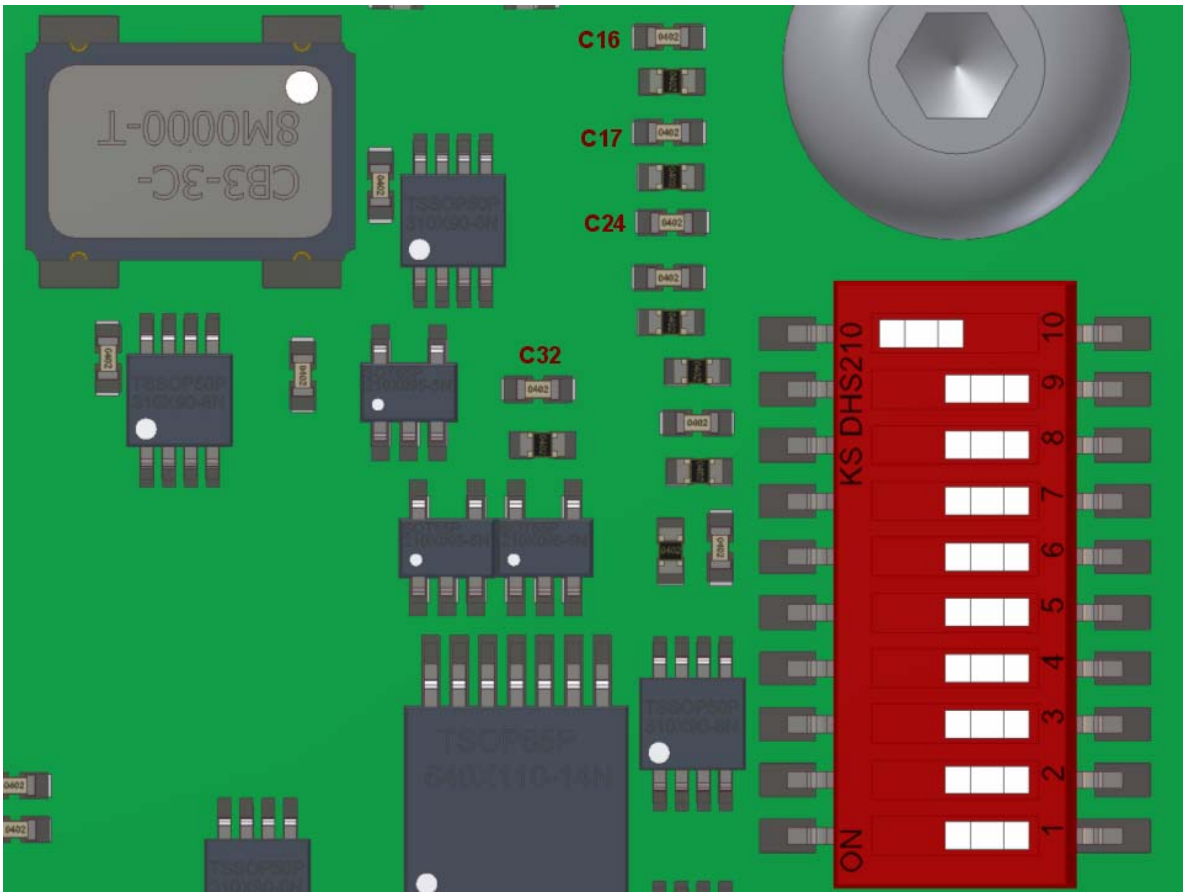


Figure D-2. Switch S2 Onboard Reset Pulse Setting.

D.2. Install a jumper across pins 3 and 4 of header H2 to enable the multifunction port H1 to accept static commands as shown in Figure D-3.

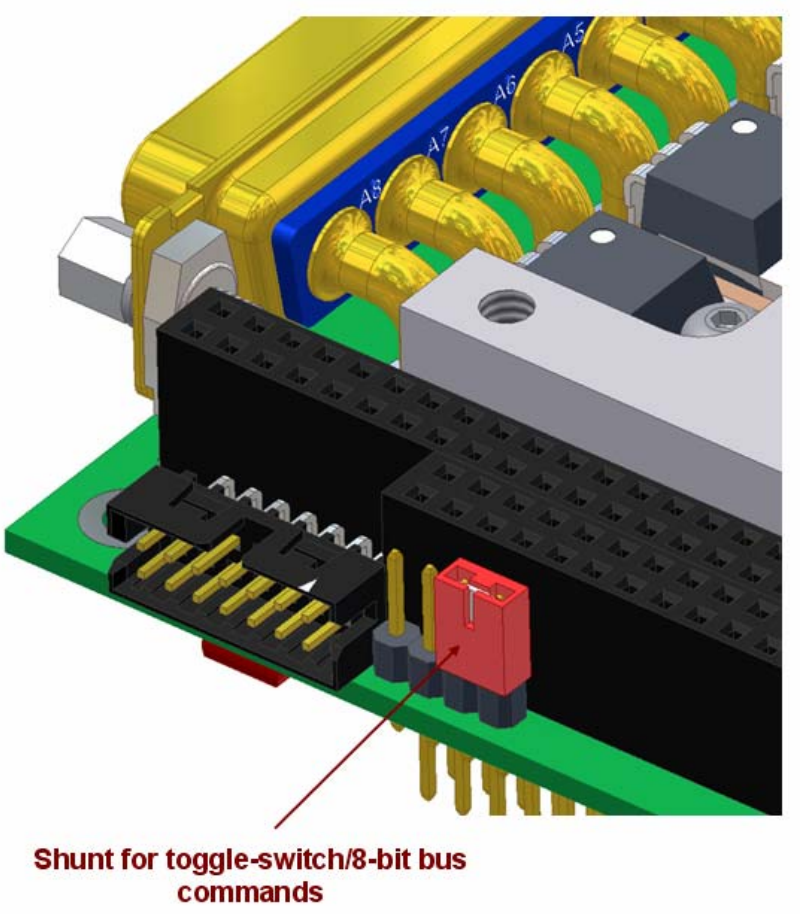


Figure D-3. H2 Jumper Position for Toggle-Switch Commands .

D.3. Verify the CPLD's DRIVER MUX is set up to select toggle-switch/8-bit bus commands by setting DIP switch S1-1 to **ON** and DIP switch S1-2 to **OFF**. See Figure D-4.

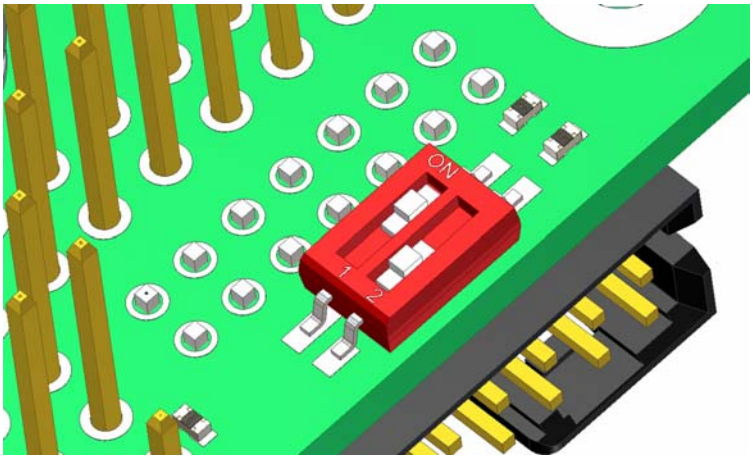


Figure D-4. S1 Configuration for Toggle-Switch/8-Bit Bus Ops.

D.4. Verify the command cable is connected between the external toggle-switches/8-bit bus and multifunction port H1.

D.5. Verify that a +5VDC supply cable has been attached to auxiliary power connector J6.

D.6. Verify that a cable has been attached to connector J1 to supply the power to be switched by MOSFET power channel 0.

D.7. Verify that the external toggle-switches are in the **OFF** position.

D.8. If an 8-bit bus is used, each of the command lines CMD7:0 should be at logic low. Control line CMDEN should also be at logic low. The strobe line CMDCK triggers the MOSFET driver latch on a rising (logic low to logic high) edge.

D.9. Switch **ON** power to the auxiliary power connector J6.

D.10. Switch **ON** the input power to MOSFET power channel 0.

D.11. If external MOSFET monitoring LEDs are used, verify that these are **OFF**.

D.12. Throw the CMD0 switch to the **ON** position (SW1 in Figure D-1). If an 8-bit bus is used instead of toggle-switches, raise the CMD0 control line to a logic high level.

D.13. The CMD0 latch is set. (MOSFET power channel 0 remains **OFF** until subsequent enable and strobe commands.) Verify CMD0 LED is **ON**.

D.14. Throw the CMDEN switch to the **ON** position (SW9 in Figure D-1). If an 8-bit bus is used instead of toggle-switches, raise the CMDEN control line to a logic high level.

D.15. The CMDEN latch is set. (MOSFET power channel 0 remains **OFF** until subsequent strobe command.) Verify CMD0 LED is **ON**.

D.16. Throw the CMDCK switch to the **ON** position and then back to the **OFF** position . (SW10 in Figure D-1). If an 8-bit bus is used instead of toggle-switches, pulse (10us min) the CMDCK control line to a logic high level and then return it to logic low.

D.17. The CMDCK command strobes the MOSFET driver latch. MOSFET power channel 0 switches **ON**. Verify CMDCK LED flashes briefly when the CMDCK toggle-switch is actuated.

D.18. To switch off MOSFET power channel 0, follow the steps outlined below.

D.19. Throw the CMD0 switch to the **OFF** position (SW1 in Figure D-1.).

D.20. The CMD0 latch is cleared. (MOSFET power channel 0 remains **ON** until subsequent strobe command.) Verify CMD0 LED is **OFF**.

D.21. Throw the CMDCK switch to the **ON** position and then back to the **OFF** position (SW10 in Figure D-1.). If an 8-bit bus is used instead of toggle-switches, pulse (10us min) the CMDCK control line to a logic high level and then return it to logic low.

D.22. The CMDCK command strobes the MOSFET driver latch. MOSFET power channel 0 switches **OFF**. Verify CMDCK LED flashes briefly when the CMDCK toggle-switch is actuated.

D.23. Switch **OFF** the input power to MOSFET power channel 0.

D.24. Switch **OFF** power to the auxiliary power connector J6.

APPENDIX E

PUSH-BUTTON OPERATION

Figure E-1 is a schematic of a possible arrangement for operating the MOSFET power channels using normally open push-button switches. For example, to switch on MOSFET power channel 0, please follow the sequence outlined below:

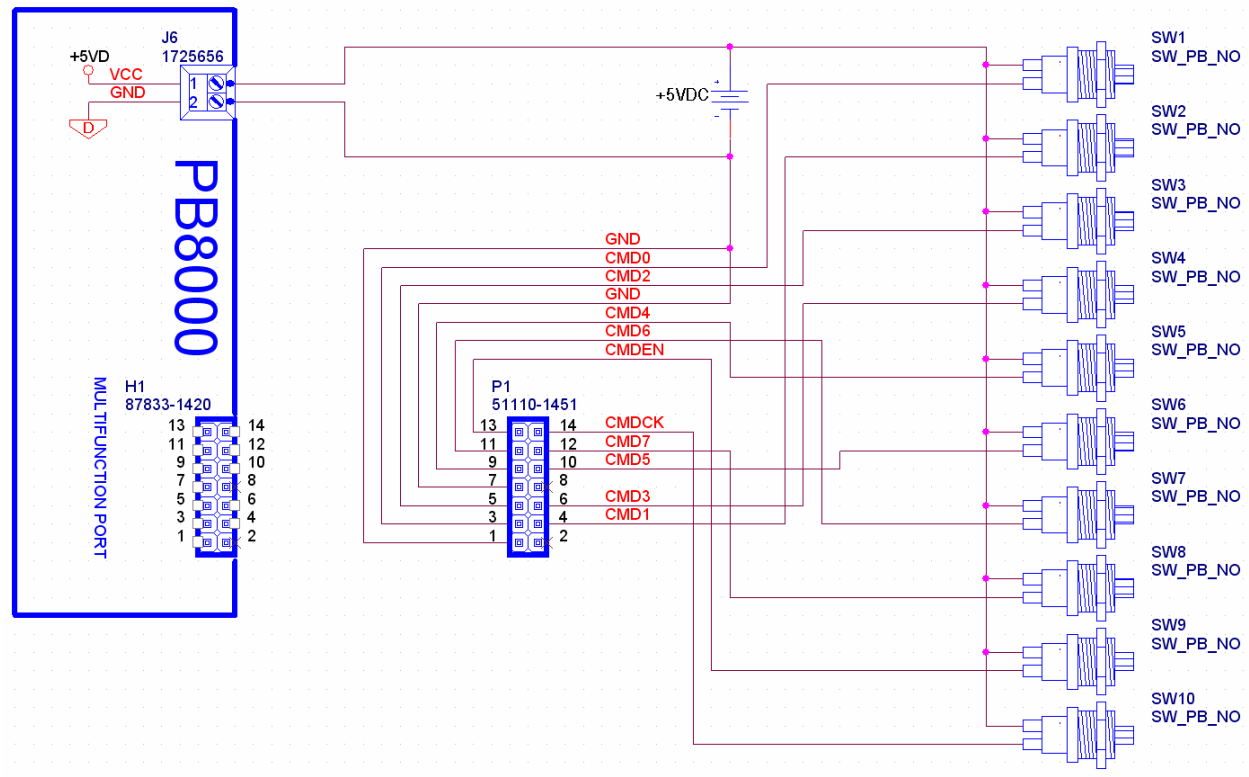


Figure E-1. Push-Button Schematic.

E.1. Note: For the pulsed commands to operate, the four RS485 terminating capacitors C16, C17, C24 and C32 must not be present. Verify that these capacitors are not installed on the board. See Figure E-2.

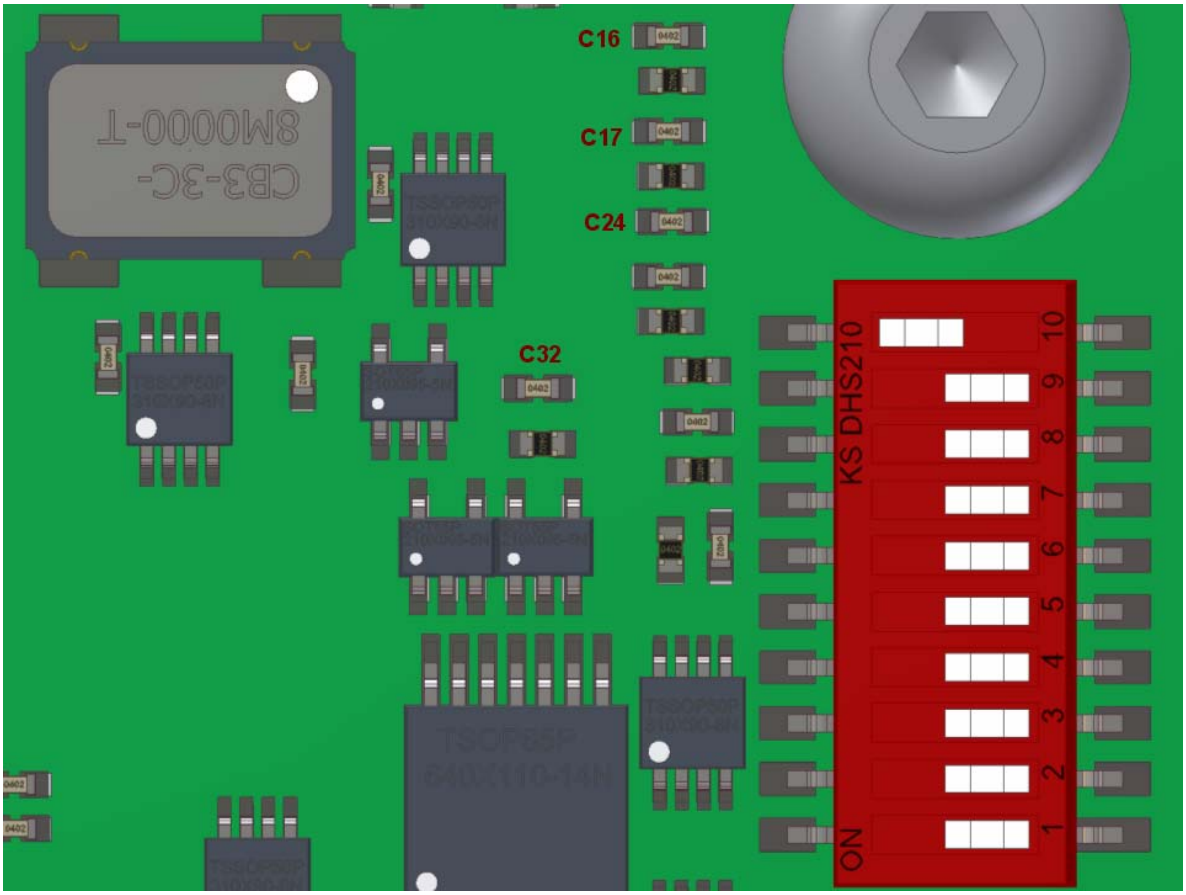


Figure E-2. RS485 Terminating Capacitors.

E.2. Configure DIP switch S2 for on-board reset pulse by setting DIP switch S2-10 to **ON**.

E.3. Verify all jumpers have been removed from header H2 to enable the multifunction port H1 to accept pulsed commands.

E.4. Verify the CPLD's DRIVER MUX is set up to select push-button commands by setting DIP switch S1-1 to **OFF** and DIP switch S1-2 to **OFF**. See Figure E-3.

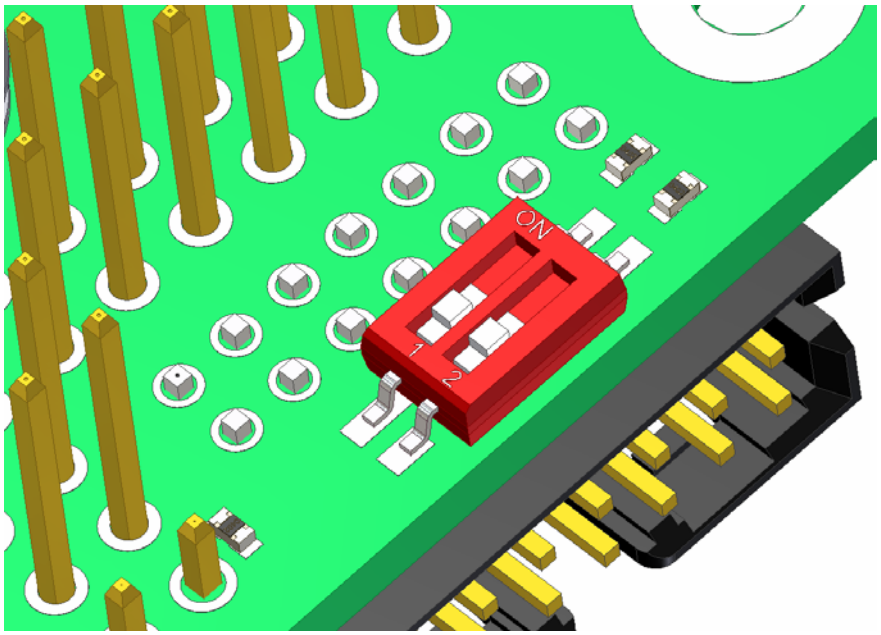


Figure E-3. S1 Configuration for Push-Button Ops.

E.5. Verify the command cable is connected between the external push-buttons and multifunction port H1.

E.6. Verify that a +5VDC supply cable has been attached to auxiliary power connector J6.

E.7. Verify that a cable has been attached to connector J1 to supply power to be switched by MOSFET power channel 0.

E.8. Switch **ON** power to the auxiliary power connector J6.

E.9. Switch **ON** the input power to MOSFET power channel 0.

E.10. Verify all MOSFET monitoring LEDs are OFF.

E.11. Depress and release the CMD0 push-button switch (SW1 in Figure E-1.).

E.12. The CMD0 command is debounced and latched. (MOSFET power channel 0 remains **OFF** until subsequent enable and strobe commands.) Verify CMD0 LED is **ON**.

E.13. Depress and release the CMDEN push-button switch (SW9 in Figure E-1.).

E.14. The CMDEN command is debounced and latched. (MOSFET power channel 0 remains **OFF** until subsequent strobe command.) Verify CMDEN LED is **ON**.

E.15. Depress and release the CMDCK push-button switch (SW10 in Figure E-1.).

E.16. The CMDCK command strobes the MOSFET driver latch. MOSFET power channel 0 switches **ON**. Verify CMDCK LED flashes briefly when the CMDCK push-button switch is depressed.

E.17. To switch off MOSFET power channel 0, follow the steps outlined below.

E.18. Depress and release the CMD0 push-button switch (SW1 in Figure E-1.).

E.19. The CMD0 command is debounced and toggles it's latch. (MOSFET power channel 0 remains **ON** until subsequent strobe command.) Verify CMD0 LED is **OFF**.

E.20. Depress and release the CMDCK push-button switch (SW10 in Figure E-1.).

E.21. The CMDCK command strobes the MOSFET driver latch and MOSFET power channel 0 switches **OFF**. Verify CMDCK LED flashes briefly when the CMDCK push-button switch is depressed.

E.22. Switch **OFF** the input power to MOSFET power channel 0.

E.23. Switch **OFF** power to the auxiliary power connector J6.